



SILICON LINK

AS2431

Precision Adjustable Shunt Reference

Features

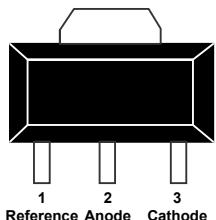
- Temperature-compensated: 15 ppm/ $^{\circ}\text{C}$
- Trimmed bandgap reference
- Internal amplifier with 100 mA capability
- Multiple temperature ranges
- Low frequency dynamic output impedance:
 $< 450 \text{ m}\Omega$
- Low output noise
- Available in Lead Free (ROHS compliant) version.

Description

The AS2431 is a three-terminal adjustable shunt regulator providing a highly accurate bandgap reference. The adjustable shunt regulator is ideal for a wide variety of linear applications that can be implemented using external components to obtain adjustable currents and voltages.
In the standard shunt configuration, the combination of low temperature coefficient (TC), sharp turn-on characteristics, low output impedance and programmable output voltage make this precision reference an excellent error amplifier. The AS2431 is a direct replacement for the AS431 in low voltage, low current applications. It is also available in the very small footprint SOT-23.

PIN CONFIGURATION – Top View

SOT-89



PACKAGE TOP MARKING:
(For SOT-89)

AS2431
YMXXXS

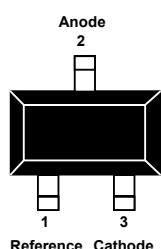
Line 1: Device

Line 2: Lot No. Code

YMXXX – 5 Character Lot No.
mark excluding 1st letter
character of lot no.

S – Split Code

SOT-23 / 3L



PACKAGE TOP MARKING:
(For SOT-23 / 3L)

BBB

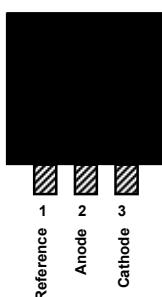
Line 1:# BBB

– Device Number
(single letter code)
BBB – Sequential Number

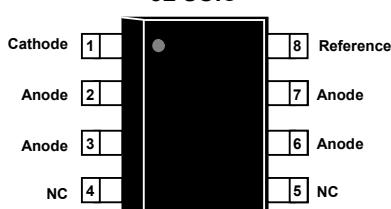
Note:

1. # is based on Silicon Link Device Marking Guidelines (refer to SLI form no. FM-40217)
2. BBB is based on Silicon Link Logbook Code

TO-92



8L SOIC



PACKAGE TOP MARKING:
(For both TO-92 & 8L SOIC)

AS2431
FYMXXXS
GYYWW

Line 1: Device

Line 2: Lot No. Code

F – Foundry Code (S)
YMXXX – 5 Character Lot No.
S – Split Code

Line 3: Date Code

G – Assembly Vendor Code
YY – Year
WW – Workweek

ORDERING INFORMATION

AS2431 B R5 D8 13

Circuit Type: _____
Precision Adjustable
Shunt Reference

Temperature Range: _____
A = 0°C to 70°C
B = 0°C to 105°C
C = -40°C to +85°C
D = -55°C to +125°C

Bandgap Tolerance: _____
2 = $\pm 2\%$ V
1 = $\pm 1\%$ V
R4 = $\pm 0.4\%$ V
R5 = $\pm 0.5\%$ V
R25 = $\pm 0.25\%$ V

Packaging Option:

A = Ammo Pack
B = Bulk
T = Tube
7 = Tape and Reel (7" Reel Dia)
13 = Tape and Reel (13" Reel Dia)

Package Style:

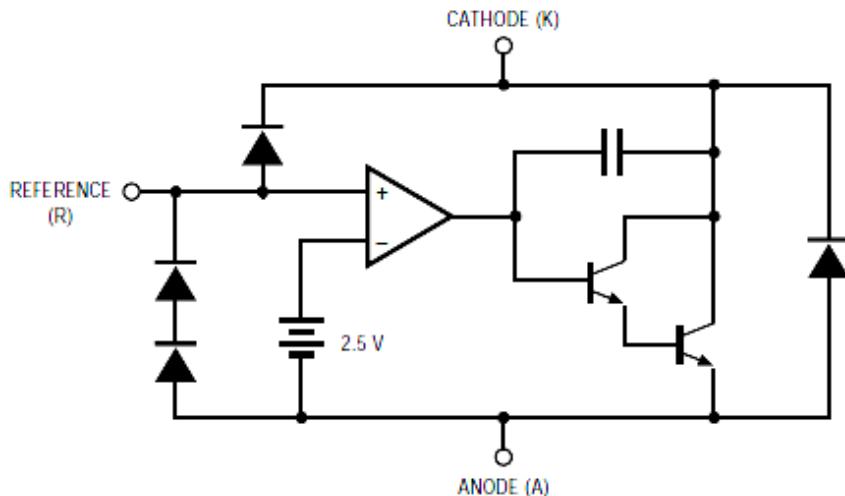
LP = TO-92
S = SOT-89
VS = SOT-23/3L
D8 = SOIC/8L



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Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Cathode-Anode Reverse Breakdown	V_{KA}	18	V
Anode-Cathode Forward Current	I_{AK}	1	A
Operating Cathode Current	I_{KA}	100	mA
Reference Input Current	I_{REF}	1	mA
Continuous Power Dissipation at 25°C	P_D		
TO-92		775	mW
8L SOIC		750	mW
SOT-89		1000	mW
SOT-23/3L		200	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	-65 to 150	°C
Lead Temp, Soldering 10 Seconds	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Conditions

Parameter	Symbol	Rating	Unit
Cathode Voltage	V_{KA}	V_{REF} to 18	V
Cathode Current	I_K	10	mA

Typical Thermal Resistances

Package	θ_{JA}	θ_{JC}	Typical Derating
TO-92	160°C/W	80°C/W	6.3 mW/°C
SOIC	175°C/W	45°C/W	5.7 mW/°C
SOT-89	110°C/W	8°C/W	9.1 mW/°C
SOT-23/3L	575°C/W	150°C/W	1.7 mW/°C



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Electrical Characteristics

Electrical Characteristics are guaranteed over full junction temperature range (0 to 105°C). Ambient temperature must be derated based on power dissipation and package thermal characteristics. The conditions are: $V_{KA} = V_{REF}$ and $I_K = 10 \text{ mA}$ unless otherwise stated.

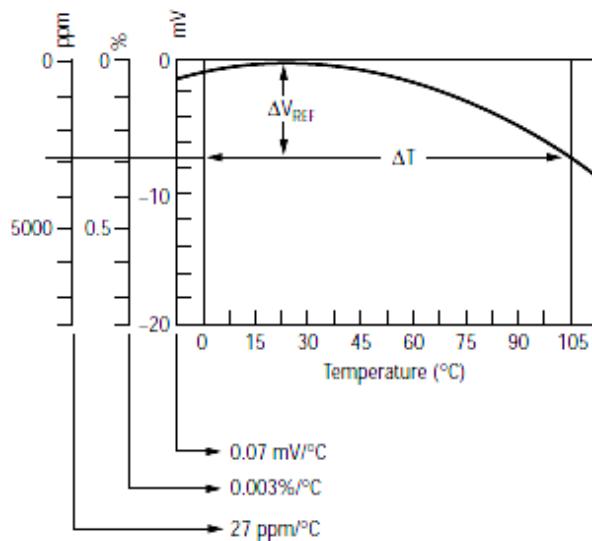
Parameter	Symbol	Test Condition	AS2431 (0.25%)			AS2431 (0.5%)			Unit	Test Circuit
			Min.	Typ.	Max.	Min.	Typ.	Max.		
Reference Voltage	V_{REF}	$T_A = 25^\circ\text{C}$	2.494	2.500	2.506	2.490	2.500	2.515	V	1
		Over temp.	2.480		2.518	2.480		2.530	V	1
ΔV_{REF} with Temp*	TC			0.04	0.06		0.04	0.06	mV/°C	1
Ratio of Change in V_{REF} to Cathode Voltage	$\frac{\Delta V_{REF}}{\Delta V_K}$	V_{REF} to 10 V	-2.7	-1.01		-2.7	-1.01		mVV	2
		10 V to 18 V	-2	-0.4	0.3	-2	-0.4	0.3		
Reference Input Current	I_{REF}			0.7	4		0.7	4	µA	2
I_{REF} Temp Deviation	ΔI_{REF}	Over temp.		0.4	1.2		0.4	1.2	µA	2
Min I_K for Regulation	$I_{K(min)}$			0.4	1		0.4	1	mA	1
Off State Leakage	$I_{K(off)}$	$V_{REF} = 0 \text{ V}$, $V_{KA} = 18 \text{ V}$		0.04	500		0.04	500	nA	3
Dynamic Output Impedance	Z_{KA}	$f \leq 1 \text{ kHz}$ $I_K = 1 \text{ to } 150 \text{ mA}$		0.45	1		0.45	1	Ω	1

Parameter	Symbol	Test Condition	AS2431 (1.0%)			AS2431 (2.0%)			Unit	Test Circuit
			Min.	Typ.	Max.	Min.	Typ.	Max.		
Reference Voltage	V_{REF}	$T_A = 25^\circ\text{C}$	2.470	2.495	2.520	2.440	2.495	2.550	V	1
		Over temp.	2.450		2.540	2.415		2.580	V	1
ΔV_{REF} with Temp*	TC			0.04	0.06		0.04	0.06	mV/°C	1
Ratio of Change in V_{REF} to Cathode Voltage	$\frac{\Delta V_{REF}}{\Delta V_K}$	V_{REF} to 10 V	-2.7	-1.01		-2.7	-1.01		mVV	2
		10 V to 18 V	-2	-0.4	0.3	-2	-0.4	0.3		
Reference Input Current	I_{REF}			0.7	4		0.7	4	µA	2
I_{REF} Temp Deviation	ΔI_{REF}	Over temp.		0.4	1.2		0.4	1.2	µA	2
Min I_K for Regulation	$I_{K(min)}$			0.4	1		0.4	1	mA	1
Off State Leakage	$I_{K(off)}$	$V_{REF} = 0 \text{ V}$, $V_{KA} = 18 \text{ V}$		0.04	500		0.04	500	nA	3
Dynamic Output Impedance	Z_{KA}	$f \leq 1 \text{ kHz}$ $I_K = 1 \text{ to } 150 \text{ mA}$		0.45	1		0.45	1	Ω	1

*Calculating Average Temperature Coefficient (TC). Refer to following page.



Average Temperature Coefficient



$$\text{• TC in } \text{mV/}^{\circ}\text{C} = \frac{\Delta V_{\text{REF}} (\text{mV})}{\Delta T_A}$$

$$\text{• TC in } \%/\text{ }^{\circ}\text{C} = \left(\frac{\Delta V_{\text{REF}}}{V_{\text{REF}} \text{ at } 25^{\circ}\text{C}} \right) \times 100$$

$$\text{• TC in } \text{ppm/}^{\circ}\text{C} = \left(\frac{\Delta V_{\text{REF}}}{V_{\text{REF}} \text{ at } 25^{\circ}\text{C}} \right) \times 10^6$$

Test Circuits

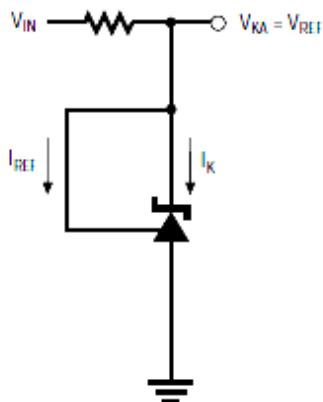


Figure 1a. Test Circuit 1

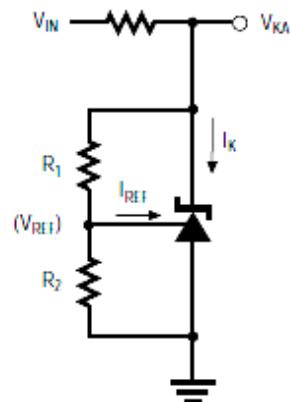


Figure 1b. Test Circuit 2

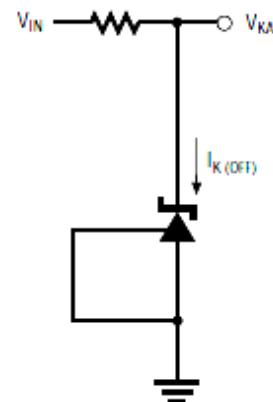


Figure 1c. Test Circuit 3



Typical Performance

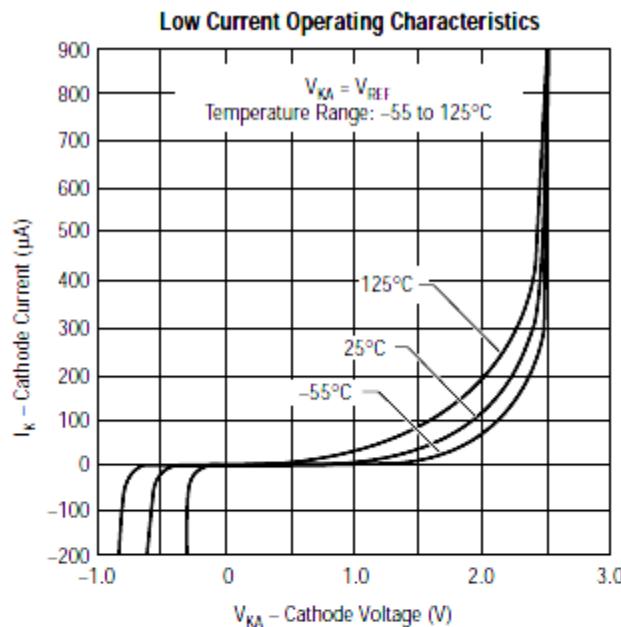


Figure 2

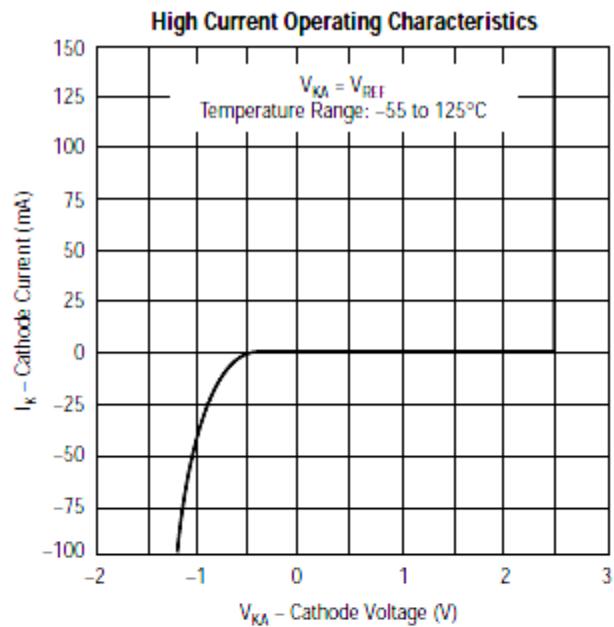


Figure 3

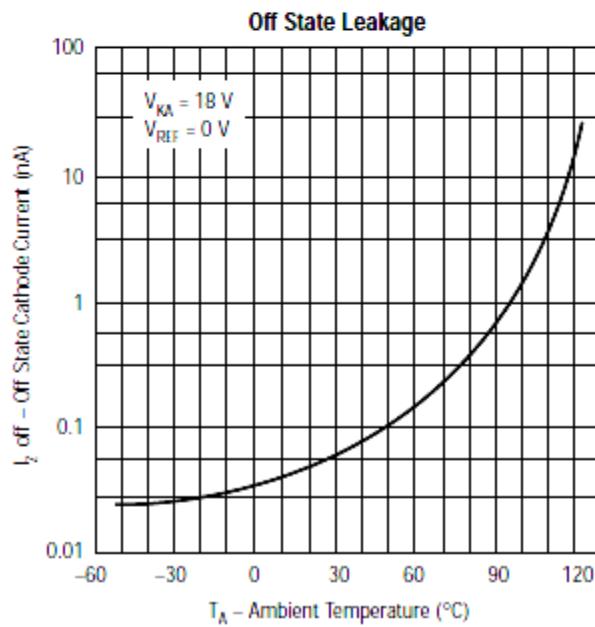


Figure 4

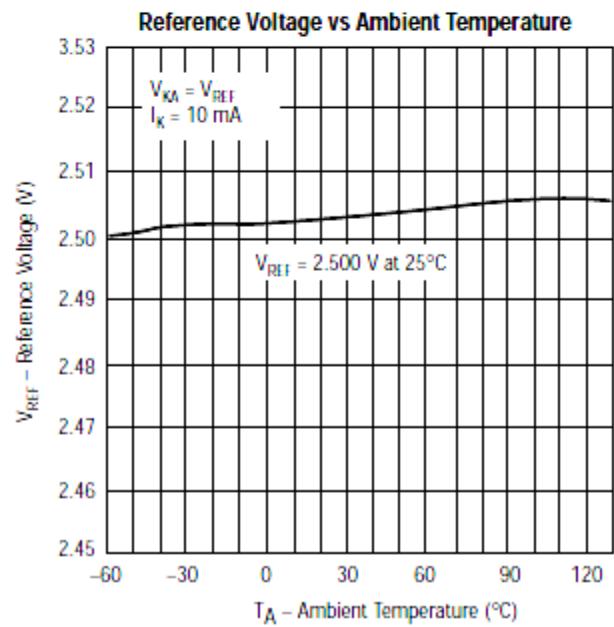


Figure 5



Typical Performance Curves

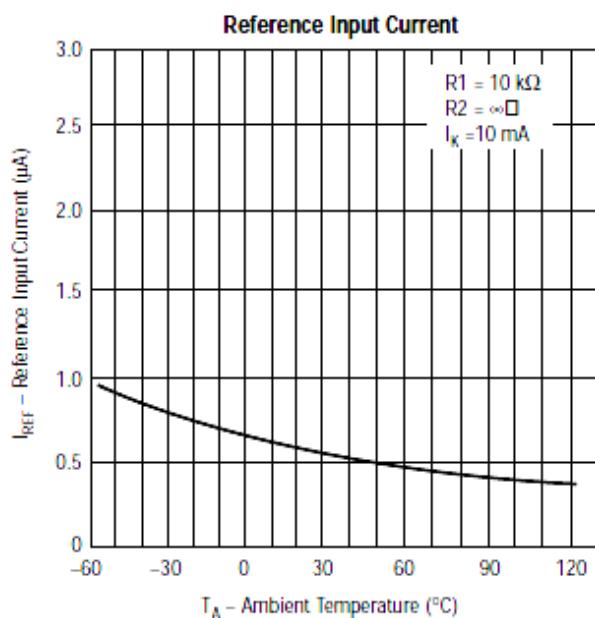


Figure 6

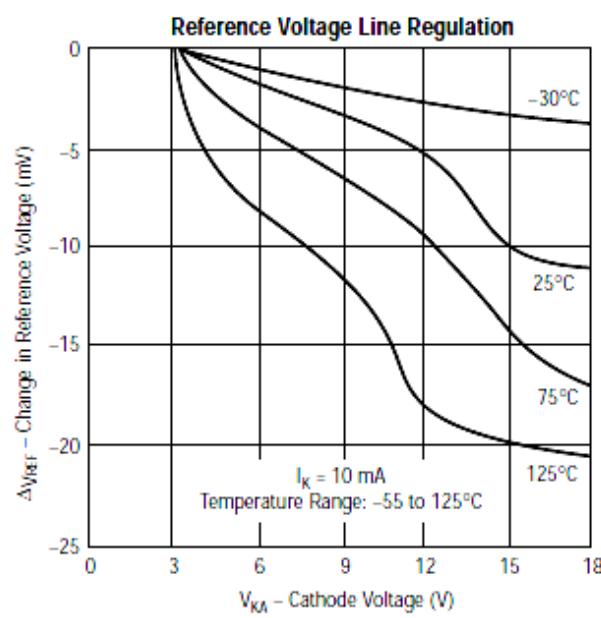


Figure 7

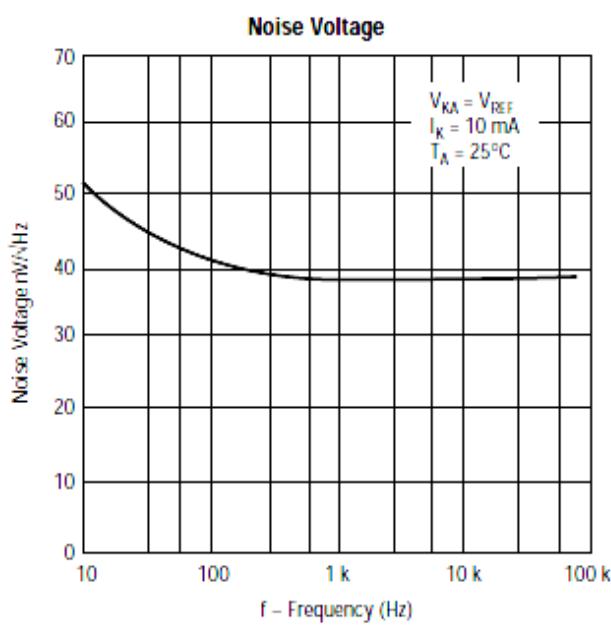


Figure 8

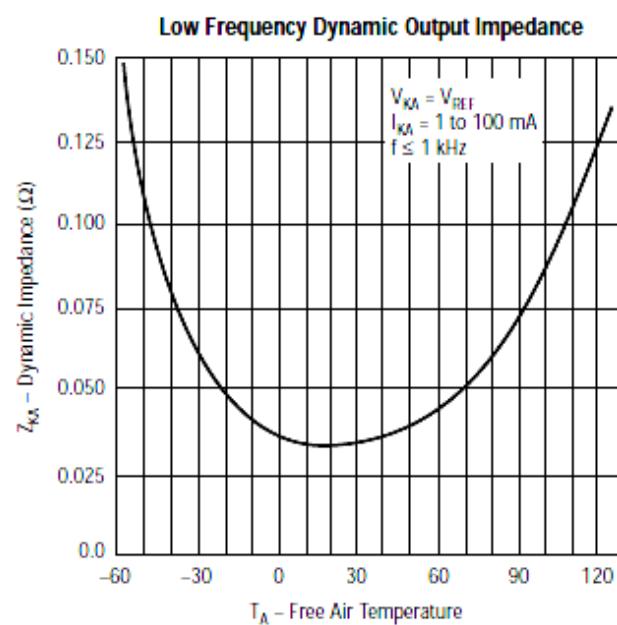


Figure 9



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Typical Performance Curves

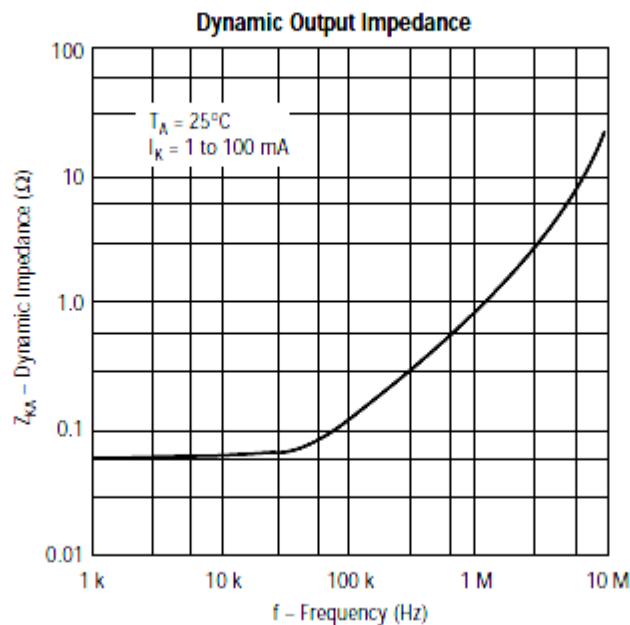


Figure 10

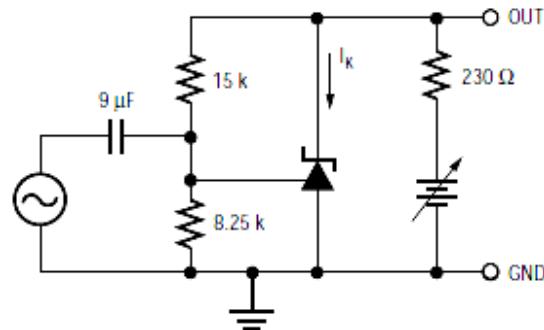
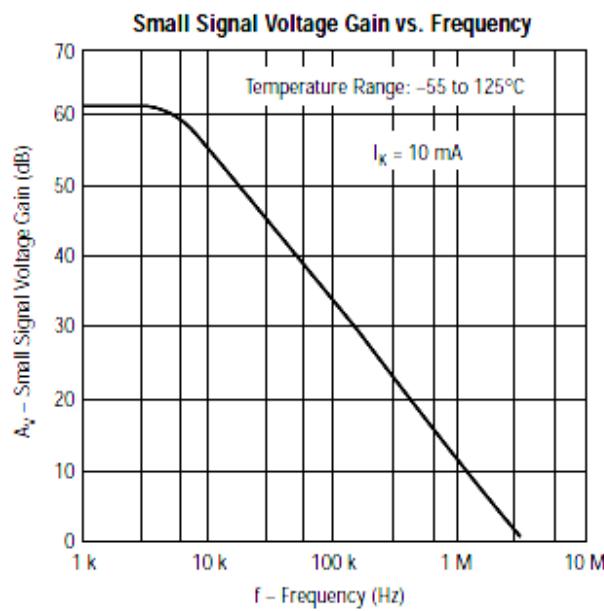


Figure 11

Typical Performance Curves

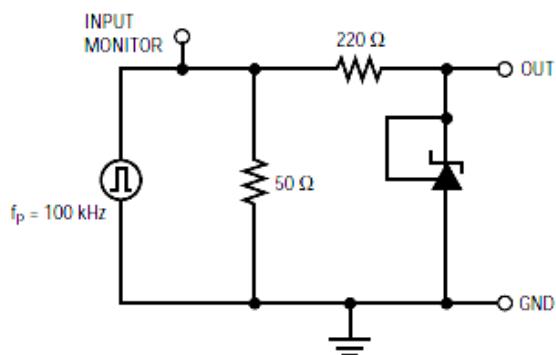
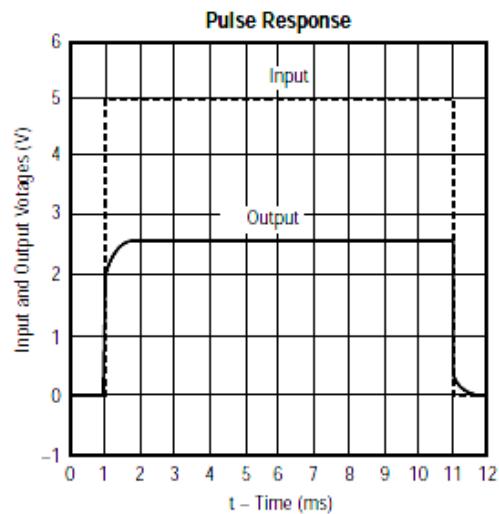


Figure 12

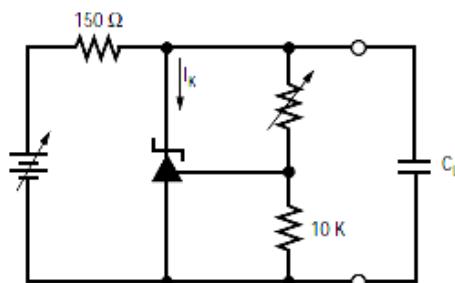
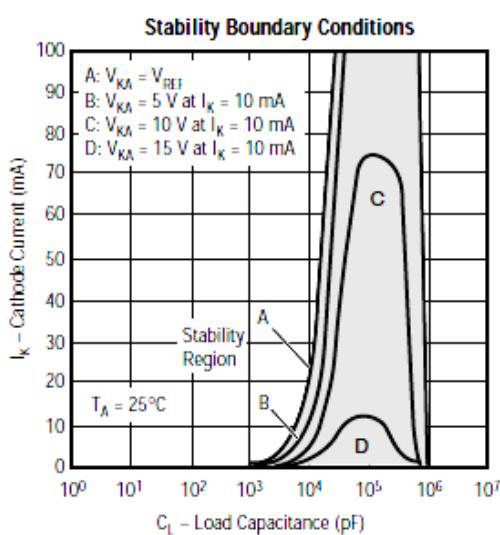
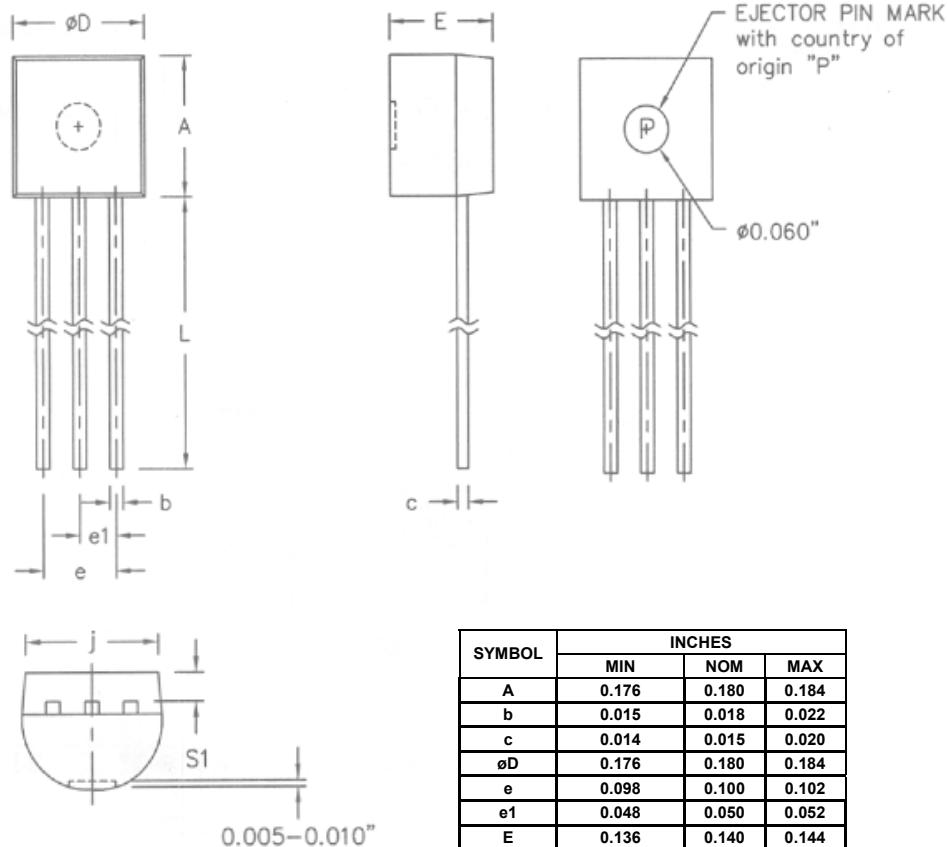


Figure 13

TO-92 PACKAGE DIMENSION

3-Lead TO-92 Plastic Package
 SLI Package Code: LP



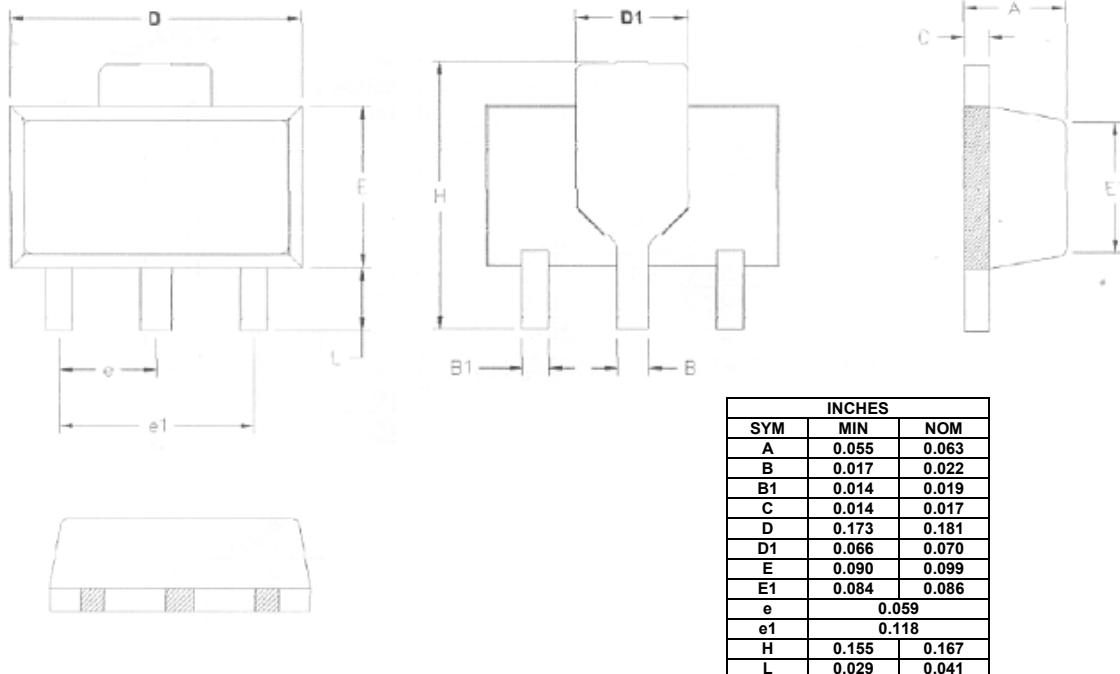
SYMBOL	INCHES		
	MIN	NOM	MAX
A	0.176	0.180	0.184
b	0.015	0.018	0.022
c	0.014	0.015	0.020
øD	0.176	0.180	0.184
e	0.098	0.100	0.102
e1	0.048	0.050	0.052
E	0.136	0.140	0.144
j	0.166	0.170	0.174
L	0.530	0.550	0.570
S1	0.031	0.035	0.039

NOTES:

1. ALL DIMENSIONS IN INCHES.
2. A MECHANICAL TOLERANCE OF $\pm 0.002"$ APPLIES TO ALL DIMENSIONS WHERE NO TOLERANCE IS EXPLICITLY GIVEN.
3. BASED FROM JEDEC TO-226 VARIATION AA OUTLINE.

SOT-89 PACKAGE DIMENSION

3-Lead SOT-89 Plastic
 Surface Mounted Package
 SLI Package Code: S



NOTES:

1. TOP PACKAGE ANGLE IS 9° +1°/-2° TOLERANCE. BOTTOM PACKAGE ANGLE IS 3° MAX.
2. PACKAGE CORNER RADIUS IS 5 MILS MAX ON ALL CORNERS.
3. SHINY PACKAGE FINISH ON ALL SIDES EXCEPT TOP SIDE FINISH IS MINIMUM MATTE OF 10-14VDI.

NOTE: ALL DIMENSION ARE IN INCHES

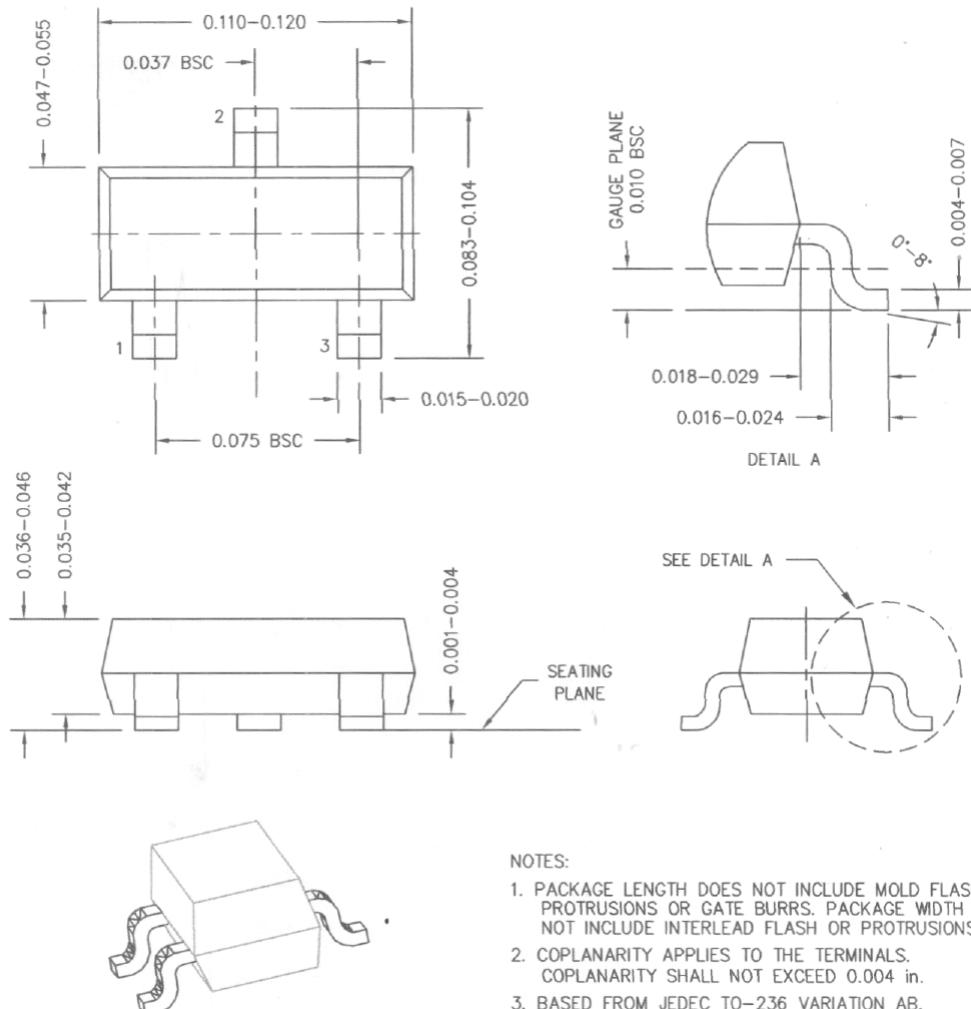


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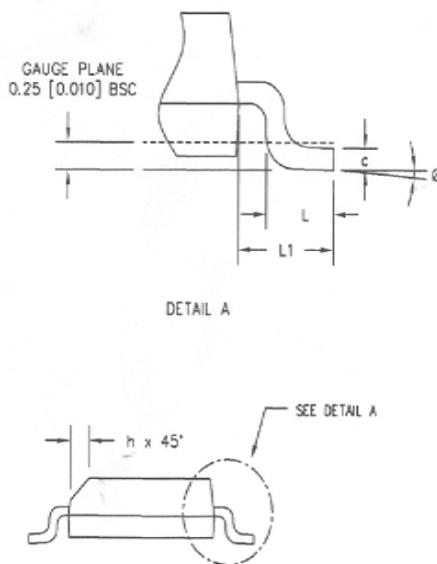
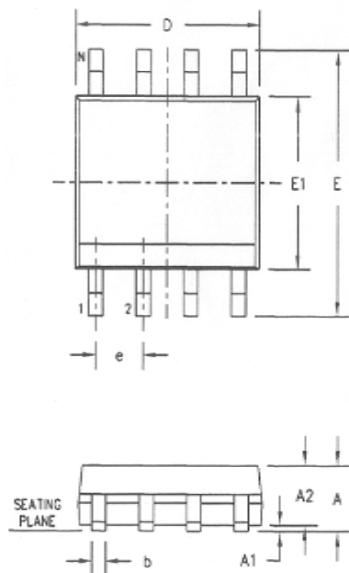
3L-SOT23 PACKAGE DIMENSION

3-Lead SOT-23 Plastic
Surface Mounted Package
SLI Package Code: VS



8L-SOIC PACKAGE DIMENSION

8-Lead SOIC Plastic
 Surface Mounted Package
 SLI Package Code: D8



SYM	DIMENSION IN INCHES			DIMENSION IN MM		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.059	0.062	0.065	1.50	1.57	1.65
A1	0.004	0.008	0.010	0.10	0.20	0.25
A2	0.051	0.054	0.057	1.30	1.37	1.45
b	0.013	0.016	0.020	0.33	0.41	0.51
c	0.007	0.008	0.010	0.18	0.20	0.25
D	0.191	0.193	0.195	4.85	4.90	4.95
E1	0.151	0.153	0.155	3.84	3.89	3.94
E	0.228	0.234	0.240	5.79	5.94	6.10
e	0.050			1.27		
L	0.020	0.024	0.032	0.51	0.61	0.81
L1	0.039	0.041	0.043	0.99	1.04	1.09
Ø	0*	-	B*	0*	-	B*
h	0.011	0.015	0.019	0.28	0.38	0.48

NOTES:

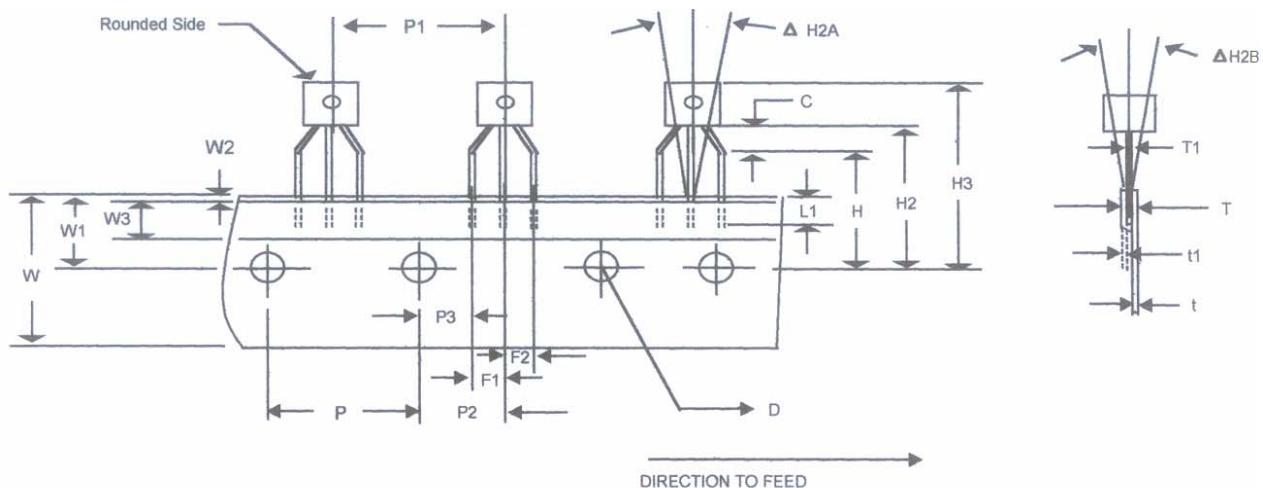
1. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
2. COPLANARITY APPLIES TO THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.003" [0.08 mm].
3. BASED FROM JEDEC NS-012 VARIATION AA.



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TO-92 AMMO PACK SPECIFICATIONS

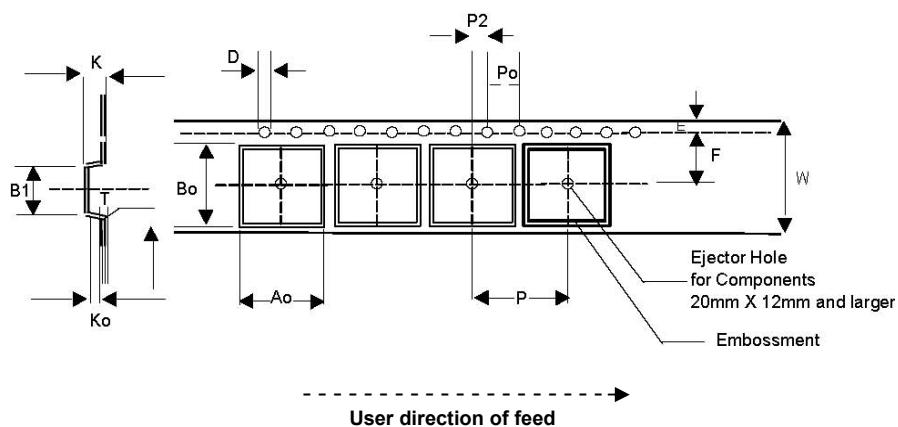


SYMBOL	DESCRIPTION	NOMINAL VALUE		TOLERANCES			
		mm	inch	mm	inch	mm	inch
D	Feed Hole Diameter	4.0	0.157	3.8	0.150	4.2	0.165
T1 (POD)	Component Lead Thickness	0.405	0.016	0.36	0.014	0.45	0.018
F1/F2	Lead Pitch (Left / Right)	2.54	0.100	2.4	0.094	2.8	0.110
C	Bottom of Component to Seating Plane	2.50	0.098	1.50	0.059	4.00	0.157
W1	Edge to Sprocket Hole Center	9.0	0.354	8.50	0.335	9.50	0.374
H2A	Deflection (Left or Right)	0.50	0.020	0	0	0.50	0.020
H2B	Deflection (Front or Rear)	1.0	0.039	0	0	1.0	0.039
H2 (H + C)	Feed Hole to Bottom of Component	18.5	0.728	17.00	0.669	20.50	0.087
H	Height of Seating Plane	16	0.630	15.5	0.610	16.5	0.650
H3	Feed Hole Center to Overall Transistor Height	27.75	1.092	23.5	0.925	32.0	1.260
L	Defective Unit Clipped Dimension	-	-	-	-	11.0	0.433
L1	Leadwire Enclosure	2.50	0.098	2.50	0.098	-	-
P	Feed Hole Pitch	12.7	0.500	12.40	0.488	13.0	0.512
P2	Center of Feed Hole to Center Lead	6.35	0.250	6.0	0.234	6.75	0.266
P3 (P2-F1)	First Lead Spacing Dimension	3.75	0.148	3.6	0.142	3.95	0.156
P1	Center Lead to Center Lead	12.7	0.500	12.2	0.500	13.2	0.520
t1	Adhesive Tape Thickness	0.18	0.007	0.16	0.006	0.20	0.008
T (t+t1+T1)	Overall Taped Package Thickness	-	-	-	-	1.55	0.061
T	Carrier Strip Thickness	0.37	0.015	0.27	0.011	0.47	0.018
W	Carrier Strip Width (18mm)	18.00	0.709	17.5	0.689	19.0	0.748
W3	Adhesive Tape Width (6mm)	6.00	0.236	5.5	0.217	6.3	0.248
W2	Adhesive Tape Position	0.25	0.010	0	0	0.50	0.020

TO-92 Ammo Pack Requirement			
Components	Tape Width (W) mm	Fan Fold Box	
TO92	3L	18	2000

PACKAGE MECHANICAL DRAWING

Surface Mountable Tape & Reel Specifications in mm (inch)
(SOIC, SOT-23 and SOT-89)



Tape Size (W)	D	E	P0	T (Max)	A0, B0, K0	T1 (Max)	Constant Dimensions
8, 12, 16, 24mm	1.55 ± 0.05 (.061±.002)	1.75 ± 0.10 (.069±.004)	4.0 ± 0.10 (.157±.004)	0.400 (.016)	See Note	0.100 (.004)	

Tape Size (W)	B1 Max.	D1 Min.	F	K Max.	P2	
8 mm	4.2 (.165)	1.0 (.039)	3.5 ± 0.05 (.138±.002)	2.4 (.094)	2.0 ± 0.05	
12 mm	8.2 (.323)	1.5 (.059)	5.5 ± 0.05 (.217±.002)	4.5 (.177)	.079±.002	Variable Dimensions

Per Package Requirement					
Components	Tape Width (W) mm	Cavity Pitch (P) mm	Devices per Reel		
			7" Reel	13" Reel	
SOIC 8L	12	8	-	2500	
SOT-23 3L	8	4	3000	-	
SOT-89 3L	12	8	-	2500	

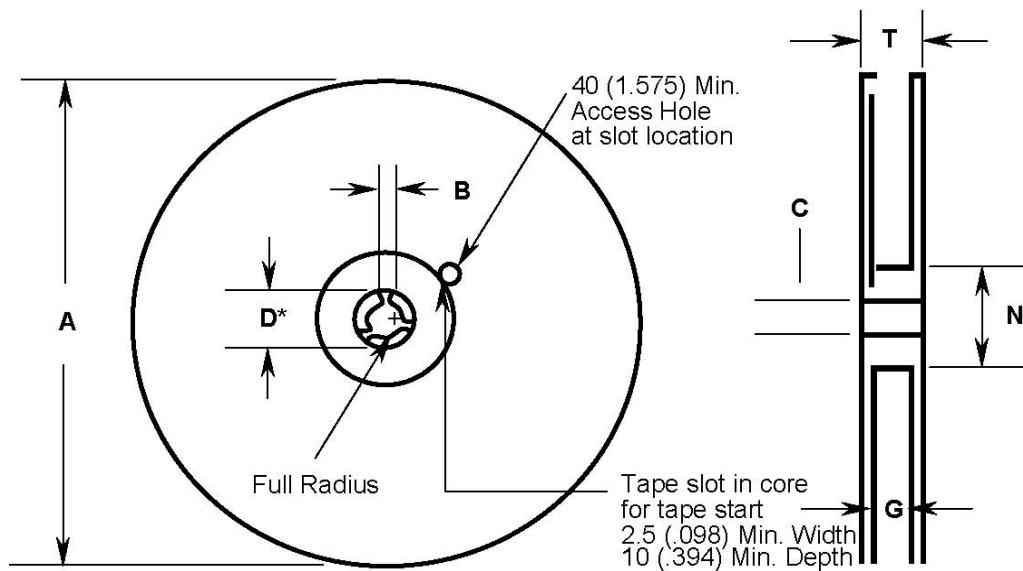
Note: Ao Bo Ko are determined by component size. The clearance between the component and the cavity must be within 0.05 [.002] min. to 0.50 [.020] max. for 8mm tape, 0.05 [.002] min to 0.65 [.026] max for 12mm tape.



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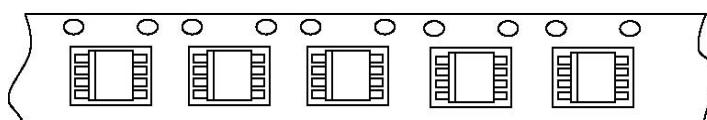
Precision Adjustable Shunt Reference



REEL DIMENSIONS							
Tape Size	A Max.	B Min.	C	D* Min.	N Min.	G	T Max.
8mm	330 (12.992)	1.5 (.059)	13.0±0.20 (.152±.008)	20.2 (.795)	50 (1.973)	8.4±1.5 0.0 (.331±.059) 0.0	14.4 (.567)
12mm	330 (12.992)	1.5 (.059)	13.0±0.20 (.152±.008)	20.2 (.795)	50 (1.973)	12.4±2.0 0.0 (.488±.078) 0.0	14.4 (.567)

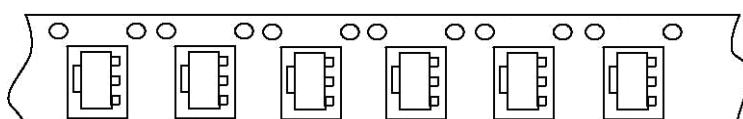
MECHANICAL POLARIZATION

SOIC-8L DEVICE



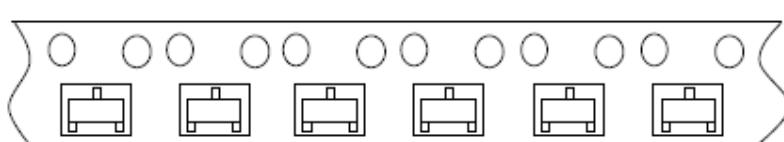
User direction of feed →

SOT-89 DEVICE



User direction of feed →

SOT-23 3L DEVICE



User direction of feed →