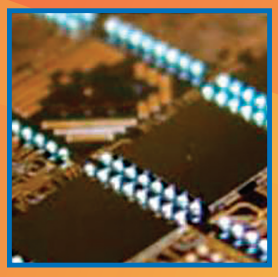
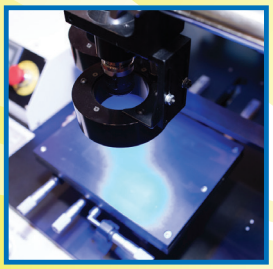
47th International Symposium on Microelectronics

October 13-16, 2014

Town & Country Resort and Conference Center • San Diego, CA







Advance Program Highlights

IMAPS 2014 Focuses on
"the Future of Packaging"
featuring that all new track!

The most **Interposer & 3D Content Under One Roof** – 6 sessions and more than 35 speakers on 3D!

Featuring keynotes from Qualcomm, Micron, Jawbone, IPDiA and IBM

The all new **Panel Discussion Thursday** on "the Future of Packaging"

19 Professional Development Courses
Monday & Thursday – all new format Monday!

28 sessions featuring more than 190 papers

2-Day Exhibition (Tues-Weds.)
with **more than 100 Exhibit Booths**

2nd Annual **"Research Lab Corridor"**
on Exhibit Floor

GBC Luncheon & Market Forum on
"Future of Packaging: Mobile & Solar PV"

"Dessert Break" in the exhibit hall
on Tuesday afternoon

Networking Reception
Wednesday evening in the Hall

Register Online: IMAPS2014.org • Early Registration & Hotel Deadline: September 12, 2014

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47th International Symposium on Microelectronics

October 13-16, 2014

Professional Development Courses (PDCs):

Monday, October 13: full-day courses, running 10:00 am - 6:00 pm (NEW HOURS);
Half-day courses (10:00am - 1:45pm & 2:15 pm - 6:00 pm)

Thursday, October 16: all half-day courses, running 8:00 am - 12:00 pm

Registration:

Atlas Foyer

Monday, October 13 – 7:00 AM - 6:00 PM
Tuesday, October 14 – 7:00 AM - 6:00 PM
Wednesday, October 15 – 7:00 AM - 5:30 PM
Thursday, October 16 – 7:00 AM - 3:30 PM

Technical Sessions:

Tuesday, October 14 – 8:00 AM - 6:25 PM
Wednesday, October 15 – 8:00 AM - 5:55 PM
Thursday, October 16 – 8:00 AM - 4:10 PM

Exhibition:

Grand Hall

Monday, October 13 – SET-UP ONLY: 9:00 AM-6:00 PM
Tuesday, October 14 – 11:00 AM - 5:00 PM
Wednesday, October 15 – 11:00 AM - 7:30 PM (NEW HOURS)
Thursday, October 16 – MOVE-OUT ONLY: 8:00 AM - 2:00 PM

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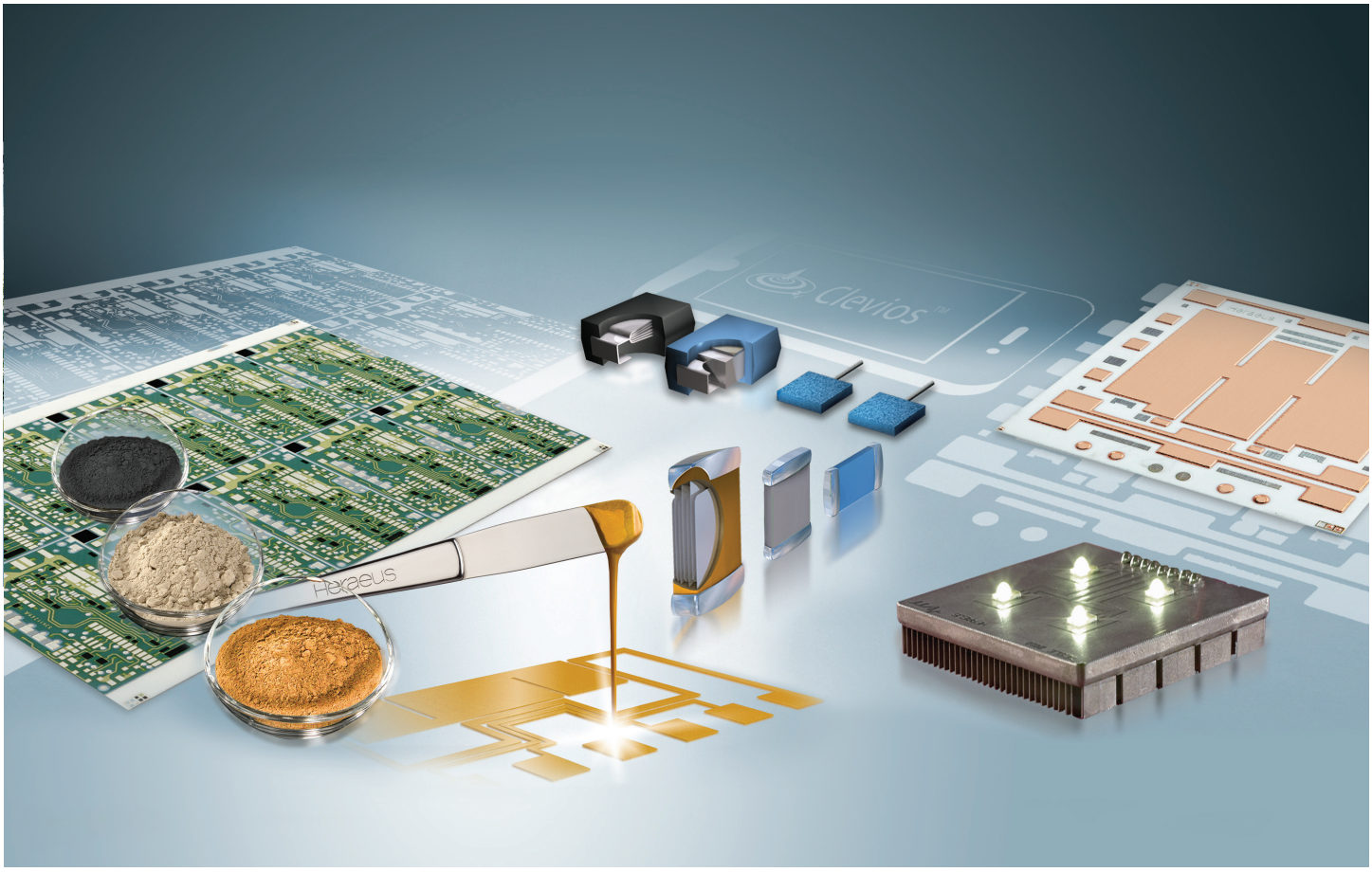

For over 40 years, Heraeus has been producing thick film pastes and LTCC materials, which are mainly used in the automotive, consumer electronics, telecommunication, LED, fuel cells and aerospace industries. The Electronic Materials Division of Heraeus specializes in materials for creating circuit elements by many production methods.

In 2010 Heraeus acquired the intrinsically conductive polymer materials – Clevios - from H.C. Stark. Since 2014 the new Circuits & Components Business Unit is responsible for thick film pastes and LTCC materials as well as conductive polymers for capacitors.

Heraeus Precious Metals, Electronic Materials Division is committed to developing new and innovative materials for the electronics market.

Heraeus' global presence and in-depth understanding of the market and technology allow us to develop customer solutions for almost any application. Our state of the art technical service laboratories ensure that these solutions work in each customer's unique processes.

It's no wonder why our products are found in such a diverse range of electronics applications and why our customers consider us their preferred partner for their critical material needs. Consider the Electronic Materials Division of Heraeus for your next material choice.

Contact: Yin Yin
Phone: +1 610 825 6050
Email: yin.yin@heraeus.com
www.thinkfilm.net

Message from the General Chair

Greetings to IMAPS members and the worldwide microelectronics community!

It's my honor to be this year's General Chair for the IMAPS 47th Annual International Symposium on Microelectronics. I hope you can join us from October 13th to 16th at the Town & Country Resort and Country Center in San Diego, CA. IMAPS 2014 promises to be a special event with a strong technical program, and a large array of technology and manufacturing vendors at the exhibition hall.

The IMAPS committees and many dedicated volunteers have enhanced the 2014 program with exciting new features that provide added international flavor, and more learning and growth opportunities for you and your business. This year's Technical Chairman, Subramanian "Subu" S. Iyer, has organized a team of co-chairs and session chairs for IMAPS 2014 and generated a strong program that will feature outstanding technical papers on the latest research, development, and product advances. Our theme this year is the "future of packaging." The technical program is organized into multiple parallel tracks covering Advanced Packaging, Interconnects & Assembly, Interposers & 2.5/3D Packaging, Modeling, Design, Test & Reliability, New Materials & Processing, as well as Emerging Technologies. Keynote speakers will be highlighted on each day of the symposium, and a panel on "the future of packaging" will provide expert insights on the latest advances in this emerging field.

Be sure to visit the Research Center corridor in the Exhibit show floor and more than 100 exhibitors who will showcase a vast array of new products serving all segments of the microelectronics industry, including Military, Aerospace, Consumer, Mobile, Biomedical, Computing, Automotive/Industrial, and Alternate Energy to find out the latest and greatest solutions to your needs in the supply chain. We will also have an outstanding lineup of Professional Development Courses and an expanded roster of market presentations at the Global Business Council Forum.

University students will have an opportunity to showcase their research and win prize money in a Student interactive poster session. And the IMAPS outreach program will facilitate a program with local high school students, giving students a chance to see what the microelectronics industry is all about. To round out the activities, a fun golf tournament will be held to help us on the "all work and no play" front.

It's been my pleasure to work with a diligent and steadfast organizing committee and IMAPS staff and a robust team of volunteers and co-chairs. They have assembled a superb program that truly brings the entire electronics supply chain together and I can't think of a better place to stay in tune than at IMAPS 2014 in San Diego. I encourage you take some time from your busy schedule to attend IMAPS 2014, to learn about a diverse scope of technology advancements, meet and collaborate with your peers, and create a network of new contacts from all over the world!

See you in San Diego!

Dr. Ivan Ndip
General Chair, IMAPS 2014

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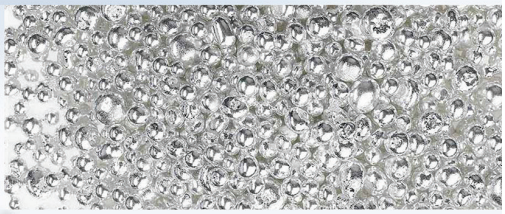

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Message from the Technical Chair

It's a really exciting and transformative time to be working in the packaging and system scaling area. This year's IMAPS 47th International Symposium on Microelectronics in San Diego promises to capture that excitement. Our theme this year is the ***"future of packaging."*** For too long, Packaging has been viewed as Silicon Technology's poor cousin, where the focus has been on doing the same thing for less. With classical silicon scaling saturating, and the cost per transistor, in some estimates potentially increasing, keeping the expectations of Moore's "law" going for another decade or two will depend on how we successfully scale packages and boards. We are beginning to see some of this new thinking in the introduction of new products that leverage interposers and 3D integration, new wearable and medical devices and the adoption of silicon and flat-panel technologies. We will capture this sentiment on Thursday's plenary session where we will hear about the packaging challenges in memory from Micron, wearables from Jawbone and medical devices from IPDiA. This will be followed by a panel discussion by industry and academic technical and business leaders on the nature, challenges and impact of this transformation.

But this year's IMAPS is a lot more! There will be multiple parallel tracks which cover developments in classical packaging, new materials, new assembly methods as well as dedicated tracks on 3D and interposers. Each day will be start off with a key note talk on the packaging in the mobile space from Qualcomm, and on panel fan-out processing from SPIL. All sessions will begin with a lead talk that will set the tone of that session.

We are also trying to post the papers on the IMAPS website so they can be accessed by attendees wirelessly on-demand both during and after the conference by registered attendees using their portable devices that they have helped build.

My co-chairs Erica Folk, Andre Rouzaud, Woong-Sun Lee, Urmi Ray, Gabriel Pares, and Yasuhiro Kawase, our track and session chairs, and our General Chair, Ivan Ndip, are working really hard to develop this into a memorable program. Details will be posted on the IMAPS 2014 website: **www.imaps2014.org**.

See you all at San Diego on October 13-16!

Dr. Subramanian (Subu) S. Iyer
Technical Chair, IMAPS 2014

IMAPS 2014 Sponsorship

All sponsorship packages can be modified at the request of companies interested in specific opportunities (if not already reserved). A la carte options can be made available upon request, or new opportunities can be created.

Contact Brian Schieman at bschieman@imaps.org or 412-368-1621 with sponsorship questions or to request a customized package.

Why you should be a Sponsor of IMAPS 2014?

- **Location - Location - Location - IMAPS 2014** will be back on the West Coast - a hot-bed for the microelectronics/packaging industries!
- You will be able to reach the niche market of microelectronic packaging professionals under one roof, many of whom are located on the West Coast, particularly Southern California.
- Keep your company's name prominent in the eyes of your peers and customers.
- Enhance your company's visibility at IMAPS 2014.
- Increase traffic to your IMAPS 2014 Exhibit Booth.

IMAPS 2014 Sponsor Benefits?

- Your company name/logo prominently displayed throughout the event in high traffic areas.
- Specialized signage at sponsored event.
- Recognition in various IMAPS publications, including the IMAPS 2014 Final Program.
- Listing as a Sponsoring Company on the IMAPS 2014 Website with a link to your website.
- Many broadcast e-mails to our address base of 20,000+.

IMAPS 2014 Sponsorship Opportunities:

PREMIER SPONSORSHIPS:

Premier Sponsor – PLATINUM | $25,000: SOLD OUT - NATEL

Includes: 20x20 "Island" Booth; Welcome Reception; Opening Ceremonies; Exhibit Hall Aisle Signs; Signage through Event; Wireless Internet Service for attendees & exhibitors in the hall Logo on Attendee Bags; Full-Day Session Sponsorship; Advance & Final Program Full-Page Advertisements; Advancing Microelectronics Magazine Advertisement; Logo on Event Website; Email Promotions; Marketing Lists; Business Meetings & Awards Ceremony Recognition; and 6 "Full Symposium" Registrations/Badges. Complimentary corporate premier membership renewal/upgrade.

Premier Sponsor – GOLD | $10,000: SOLD OUT - HERAEUS

Includes: 10x20 Booth; Welcome Reception; Opening Ceremonies; PDC Breaks/Lunch; Signage through Event; Logo Pads/Pens for all Sessions (provided by Sponsoring Company); Logo on special Key Cards for Host Hotel (provided by Sponsoring Company); Logo on Attendee Bags; Full-Day Session Sponsorship; Advance & Final Program Full-Page Advertisements; Advancing Microelectronics Magazine Advertisement; Logo on Event Website; Email Promotions; Marketing Lists; Business Meetings & Awards Ceremony Recognition; and 4 "Full Symposium" Registrations/Badges.

Premier Sponsor – SILVER | $10,000: SOLD OUT - METALOR

Includes: 10x20 Booth; Welcome Reception; Opening Ceremonies; International Reception; Badge Lanyards featuring Logo for all Attendees; Signage through Event; Logo on Attendee Bags; Full-Day Session Sponsorship; Advance & Final Program Full-Page Advertisements; Advancing Microelectronics Magazine Advertisement; Logo on Event Website; Email Promotions; Marketing Lists; Business Meetings & Awards Ceremony Recognition; and 4 "Full Symposium" Registrations/Badges.

CORPORATE SPONSORSHIPS (3 Maximum):

Corporate Sponsor | $8,500:

Includes: 10x20 Booth; Co-Sponsorship of ONE of the following: Refreshment Breaks, NEW "Dessert Hour" in the Exhibit Hall, Wednesday Exhibit Hall Lunch, OR Wednesday Exhibit Hall Reception; Signage through Event; Advance & Final Program Half-Page Advertisements; Advancing Microelectronics Magazine Half-Page Advertisement; Logo on Event Website; Web Advertisement on Event Website (and additional imaps.org pages); Email Promotions; Marketing Lists; and 3 "Full Symposium" Registrations/Badges. [Can select SOLE Sponsorship of one of the events listed above for an additional $1,500 - $10,000 total package]

"A LA CARTE" / EVENT SPONSORSHIPS:

Exhibit Hall Reception
$10,000 (Sole Sponsor) | $2,000 (Co-Sponsors – 5 Maximum):

Includes: Signage through Event; Logo on Event Website; Final Program recognition; Advance Program recognition; Recognition/Signage during Wednesday Reception; Post event attendee list; Logo Napkins provided at all food/beverage settings; Optional Drinking Glass (Beer, Wine, etc) give-away to all attendees at Reception (provided by Sponsoring Company). Sole Sponsorship includes one 10x10 booth.

Exhibit Hall Lunch
$10,000 (Sole Sponsor) | $2,000 (Co-Sponsors – 5 Maximum):

Includes: Signage through Event; Logo on Event Website; Final Program recognition; Advance Program recognition; Recognition/Signage during Wednesday Lunch; Post event attendee list; Logo Napkins provided at all food/beverage settings; Optional give-away to all attendees at lunch (provided by Sponsoring Company. Examples: logo coffee mug, drinking glass, etc).
Sole Sponsorship includes one 10x10 booth.

"Dessert Hour" in Exhibit Hall | $10,000 (Sole Sponsor All)
$2,000 (Co-Sponsors – 5): 4 AVAILABLE – 1 SOLD TO PALOMAR TECH.

Includes: Signage through Event; Logo on Event Website; Final Program recognition; Advance Program recognition; Recognition/Signage during Break(s); Logo Napkins provided at all food/beverage settings; Post event attendee list. Sole Sponsorship includes one 10x10 booth.

Conference Proceedings on USB Drive for all Full Attendees
$6,000: SOLD OUT – INDIUM CORPORATION

Includes: Sponsor Logo on USB drives distributed to all full attendees; Signage through Event; Logo on Event Website; Advance & Final Program recognition; 1 "full conference" registration; ½ Page Advertisements in Advance & Final Programs; Flyer distributed to attendees; Post event attendee list

"IMAPS Café" – Refreshments (2 Daily)
$5,000 (Sole Sponsor All) | $1,500 (Co-Sponsors – 4):
SOLD OUT – INVENSAS CORP.

Includes: Signage through Event; Logo on Event Website; Final Program recognition; Advance Program recognition; Recognition/Signage during Break(s); Logo Napkins provided at all food/beverage settings; Post event attendee list

Student Programs | $5,000:

Includes: Sponsorship of Student Industry Panel with opportunity to talk to student audience; Student Reception; Company-named Student "Best Paper" awards ($1000 1st place, $500 2nd place, $250 3rd place); $250 travel stipends to up to 10 student speakers at conference (first-come-first-serve); Logo on Event Website; Final Program recognition; Advance Program recognition; Post event attendee list

GBC Panel Discussion & Luncheon
$5,000 (Sole Sponsor) | $1,000 (Co-Sponsors – 5 Maximum):

Includes: GBC Panel & Luncheon; Signage through Event; Logo on Event Website; Advance & Final Program recognition & ¼ Page Advertisements; Company Logo on screen at opening of Panel & Lunch; 4 Seats for Lunch; Post event attendee list

Cell Phone & Device Charging Stations
$4,000 (All 3 Stations) | $1,500 (1 Station):

Includes: Mobile Device charging stations; Signage through Event; Logo on Event Website; Advance & Final Program recognition; Post event attendee list

Keynote Presentations
$2,500 (Sole Sponsor) | $1,500 (Co-Sponsors – 3 Maximum):

Includes: Signage through Event; Logo on Event Website; Advance & Final Program recognition; Company Logo on screen at opening of each Keynote; option for sponsor to introduce speaker(s); Post event attendee list.

Attendee Bag Inserts | $500 (5 Maximum):
4 AVAILABLE – 1 SOLD TO PLASMA THERM

Includes: Logo on Event Website; Advance & Final Program recognition; One (1) piece of promotional material/flyer placed in all attendee bags (printed matter provided by Sponsor); Post event attendee list

FOUNDATION GOLF SPONSORSHIPS:

Foundation Golf Invitational – "Eagle Sponsor" | $3,000:

Includes: Company Logo/Name displayed during any meals/receptions/registration at course; Entrance of 2 four-somes; Three hole sponsorships with signage; Logo on Event Website; Final Program recognition; Advance Program recognition; "Give-Aways" (provided by Sponsor)

Foundation Golf Invitational – "Birdie Sponsor" | $1,500:

Includes: Company Logo/Name displayed during registration at course; Entrance of 1 four-some; One hole sponsorship with signage; Logo on Event Website; Final Program recognition; Advance Program recognition; "Give-Aways" (provided by Sponsor)

Foundation Golf Invitational – "Hole Sponsor" | $500:

Includes: Entrance of 1 golfer; One hole sponsorship with signage; Logo on Event Website; Final Program recognition; Advance Program recognition

Foundation Golf Invitational – "Hole Sponsor" (with four-some) | $750:

Includes: Entrance of 4 golfers; One hole sponsorship with signage; Logo on Event Website; Final Program recognition; Advance Program recognition

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Exhibitors

As of June 20, 2014

Accu-Tech Laser Processing, Inc.
AdTech Ceramics
Advanced Dicing Technologies
Advantest Corporation
AI Technology, Inc.
AMICRA Microtechnologies GmbH
ASM Pacific Technology, Ltd.
ATV Technologie GmbH
Azimuth Electronics, Inc.
Besi North America, Inc.
Cleanlogix LLC
Conductive Containers, Inc.
CVInc
Deweyl Tool Company, Inc.
East China Research Institute of Microelectronics
Electronic Production Partners GmbH
Element Six Technologies US Corp.
Epoxy Technology, Inc.
ESL ElectroScience
F & K Delvotec, Inc.
Finetech, Inc.
FRT of America, LLC
Gannon & Scott
Geib Refining Corporation
Gel-Pak/Quik-Pak
Haiku Tech, Inc.
Harrop Industries, Inc.
Hary Manufacturing Incorporated
HD Microsystems
Heraeus Thick Film Division
Hesse Mechatronics, Inc.
Hi-Rel Laboratories, Inc
i3 Electronics (formerly Endicott Interconnect Technologies)
Indium Corporation
Infinite Graphics
Inkron Ltd.
Interconnect Systems, Inc.
Kulicke & Soffa Industries, Inc.
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Micross Components
Mini-Systems, Inc.
Micro Systems Technologies
MRSI Systems LLC
NAMICS Corporation
Natel Electronic Manufacturing Services, Inc.
Neu Dynamics Corp.
NorCom Systems, Inc.
Nordson DAGE
NTK Technologies, Inc.
Palomar Technologies, Inc.
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Riv, Inc.
Royce Instruments, Inc.
Rudolph Technologies
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Samtec, Inc.
SANTIER Thermal Management Solutions
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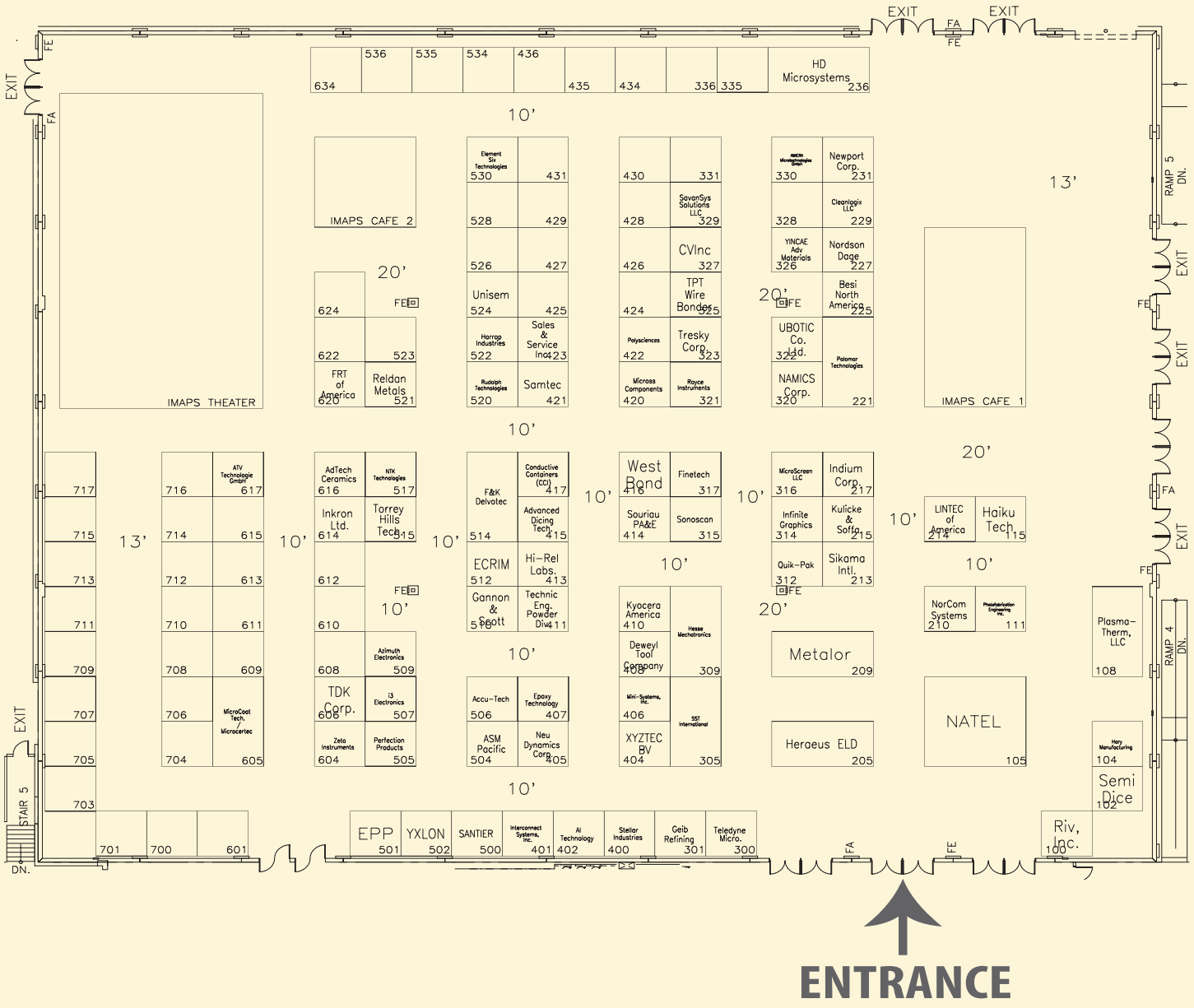
Souriau PA&E
SST International
Stellar Industries Corp.
TDK Corporation
Technic, Inc.
Teledyne Microelectronic Technologies, Inc.
Torrey Hills Technologies, LLC
TPT Wire Bonder
Tresky Corporation
UBOTIC Company Ltd.
Unisem Group
UTZ Technologies
West Bond, Inc.
XYZTEC
YINCAE Advanced Materials, LLC.
YXLON International, Inc.
Zeta Instruments

For questions or to submit booth applications (via email), contact Brian Schieman, bschieman@imaps.org, or 412-368-1621.

Exhibit Floorplan



Professional Development Courses (PDCs)

Get off line and learn Face to Face...Sign up for a PDC!

PDCs (Professional Development Course) are a big part of the Annual IMAPS Symposium each year. Why not plan to take a course on Monday or a Thursday AM session and take advantage of the rich learning opportunities available at the IMAPS symposium. This year the Monday courses are going to have a delayed start kicking off at 10 AM and running till 6 PM with a working lunch. It's something new and we hope you like it. This new time slot will give the locals a chance to beat the traffic and a little extra time for the out of town folks to get organized and prepare for a full day of learning.

PDCs create a unique environment whereby students can personally interact with the instructors, and with each other in the classroom and over lunch. It's mentally stimulating and the new found professional connections will prove to be valuable in the long run. Learning on line is fine, but it cannot duplicate eight hours spent immersed in a specific topic, led by an industry expert in the field and surrounded by like minded professionals. My father used to say, "it's not what you say but how you say it". So much of what we learn is contained in the tone of voice and non–verbal cues. PDCs provide that learning environment that's just not available on line.

This year we've put together another impressive assortment course options Our goal is to make the IMAPS PDCs the premier learning experience; so we ask that you take time to fill out the evaluation form that accompanies each course and give us your feedback on this or any other aspects of the PDCs. Read through the course descriptions on line and pick the course that best suits your company and career objectives. Every PDC includes a full set of comprehensive course notes. Class sizes typically range from eight to twenty students and there is always ample time for questions. We hope you will consider joining us in San Diego for a learning experience like no other.

Education is a lifelong pursuit, don't miss out on this opportunity!

Tom Green and James McEwen
2014 PDC Co-Chairs

Do you want to broaden and strengthen your skills and knowledge, optimize your manufacturing processes, and integrate the latest advances in materials and technologies to maintain your strength in today's competitive global market? The Technical Committee of IMAPS is pleased to present a comprehensive offering of Professional Development Courses that provide detailed information on topics of immediate interest to the Microelectronics and Packaging community. So please be sure to choose from the 19 in-depth Professional Development Courses taught by recognized industry experts. You will discover the following key ways that will benefit you.

- **Better understand the skills and knowledge necessary in today's industry.**
- **Be exposed to the rapidly expanding developments in new materials and technologies.**
- **Consult with renowned authorities about your current R&D or manufacturing problems and challenges.**
- **Learn new ways to identify, think about, and address your problems and opportunities.**
- **Great opportunities to interact with industry experts and other course attendees.**
- **Courses now offered Monday and Thursday so you can attend a course without missing the conference or extending your travel plans!**

NEW PDC FORMAT - Monday & Thursday Courses

Monday, October 13: full-day courses, running 10:00 am - 6:00 pm;
Monday, Half-day courses running 10:00am - 1:45pm & 2:15 pm - 6:00 pm

All Thursday, October 16 are half-day, running 8:00 am - 12:00 pm

MONDAY FULL-DAY PDCs: (10am-6pm)

- Introduction to 3D Printed Power Electronics & Wide Bandgap Power Semiconductor Packaging;
- Introduction to the Design and Fabrication of RF, High Speed and Microwave Hybrids, MCM's and Modules;
- Introduction to Microelectronics Packaging;
- Polymer Challenges in Electronic Packaging Including 2.5D and 3D Integration;
- Technology of Screen Printing;
- Wire Bonding

Monday PDC Lunch sponsored by:

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MONDAY MORNING HALF-DAY PDCs: (10am-1:45pm)

- ENIG - Electroless Nickel & Immersion Gold Plating for Electronics: From the Plating Solutions to the Equipment;
- High-Temperature Electronics;
- MEMS and nanoMEMS Devices and Applications;
- Package level integration : 2-D, 2.5-D and 3-D, Impact on Mobile Systems

MONDAY AFTERNOON HALF-DAY PDCs: (2:15pm-6pm)

- Low-Temperature Electronics;
- Package on Package Technology - What It Is, What Works, What Doesn't Work;
- Thermal And Mechanical Simulation Techniques For IC Package Yield, Reliability And Performance

THURSDAY HALF-DAY PDCs: (8am-12pm)

- Chip Packaging Processes and Materials;
- Fundamentals of Microelectronics Packaging;
- IC Fabrication and Electronic Packaging;
- Interposers - Silicon, Organic and Glass;
- Packaging and Testing of Implanted Medical Devices;
- Understanding the Common Failure Modes from a Physics of Failure Perspective

Your PDC Registration Fee Includes:

- "Working Lunch" (box lunch in PDC room) on the day of your course (Monday full-day PDCs only)
- Refreshment breaks
- Hard-copy workbook of course materials (no electronic copies provided)
- Attendee list following your course

PDCs under SESSIONS during IMAPS 2014 Online Registration

PDC Cancellation policy: IMAPS reserves the right to cancel a course if the number of attendees is not sufficient. You can transfer to a different course or we will refund you the corresponding amount.

Monday, October 13, 2014

Full-Day PDCs run 10:00 am - 6:00 pm
MORNING Half-Day PDCs run 10:00 am - 1:45 pm
AFTERNOON Half-Day PDCs run 2:15 pm - 6:00 pm

PDC "Working Lunch" for Full & Morning Classes: 12:00-1:00pm (Pickup box lunch & return to room)
PDC Afternoon Coffee Break in Salon Foyer: 3:30-3:45pm

PDC Coffee Breaks & Lunch sponsored by:

Heraeus

MONDAY FULL-DAY PDCs: (10am-6pm)

- Introduction to 3D Printed Power Electronics & Wide Bandgap Power Semiconductor Packaging;
- Introduction to the Design and Fabrication of RF, High Speed and Microwave hybrids, MCM's and Modules;
- Introduction to Microelectronics Packaging;
- Polymer Challenges in Electronic Packaging Including 2.5D and 3D Integration;
- Technology of Screen Printing;
- Wire Bonding

M1: Introduction to 3D Printed Power Electronics & Wide Bandgap Power Semiconductor Packaging
PDC Instructor: Douglas C Hopkins, North Carolina State University

$600 (on/before 9/12/2014); $700 (after 9/12/2014)

Course Description: Power densities and switching speeds in power electronics applications have increased well over ten fold in the last three years. With the advent of post-silicon power devices, i.e. SiC, GaN and GaAs, voltages and current densities are at unprecedented levels. The greatest change is in switching speeds that approach gigahertz. All this, and operating temperatures are pushing above 250C.

This course is an excerpt from a 45-hour university graduate course that introduces the evolving characteristics of the post-silicon devices; new "energy electronics" packaging materials; and new 3D printed power-packaging technologies. This daylong course presents a comprehensive approach from defining the new challenges facing power packaging to new packaging techniques for working at higher temperatures,

Half the course details more traditional power packaging techniques, such as directed-bonded-metal (Al - DBA and Cu - DBC) and limitations on their applicability to the new higher temperatures and speeds. The other half shows how microelectronics packaging technologies, such as 3D printing, and stack die and stacked boards, can be used in power applications for point of load converters, etc.

Who Should Attend? This course is focused toward packaging design engineers that must integrate power into digital and datacomm systems, or must create next-generation power modules.

Dr. Douglas Hopkins *is Professor and Director of the Laboratory for "˜Packaging Research in Electronic Energy Systems" as part of the NSF-funded FREEDM Systems Center at North Carolina State University in Raleigh, NC. He was formerly with SUNY Buffalo as Director of the "Electronic Power and Energy Research Lab". He received his Ph.D. from Virginia Tech, worked for GE's and Carrier's R&D Centers, and held visiting positions at several national labs. He is an IEEE senior member and IMAPS fellow. He is a founding member of IMAPS Subcommittee on Power Packaging, now chairs the technical subcommittee on Electronic Energy Packaging in IEEE-CPMT and member of the IEEE-PELS technical committee on Emerging Technologies. He has authored over 100 journal and conference publications, received three ISHM/IMAPS awards.*

M2: Introduction to the Design and Fabrication of RF, High Speed and Microwave Hybrids, MCM's and Modules

PDC Instructor: Tom Terlizzi, GM Systems IIC/Agile Microwave Technology Inc.

$600 (on/before 9/12/2014); $700 (after 9/12/2014)

Course Description: The course presents electrical and physical design, manufacturing, materials, quality and reliability information in terms understandable to engineering and non-engineering personnel. RF Packaging history, characteristics and drivers will be outlined. Types of packages (IC, chip scale, MEMS, Hybrid, MCM, Flip Chip, BGA, Aluminum and Kovar housings) and substrates (Thick and thin film, HTCC, LTCC ceramic, organic) and critical differences among them and their High Frequency applications (Microstrip, Stripline, Coplanar will be discussed. RF and Microwave layout and the commonly used design tools and software will be outlined. The course will look at the design selection to meet use and application environments. Step-by-step manufacturing flow for different packages and products will be presented as an example to understand the complexity of processes, materials and equipment involved in their manufacture. RF & Microwave packaging concepts will be introduced and the tradeoffs of different interconnect methodology (connectors, wire bonds, ribbon bonds, AuSi & AuSn eutectic, soft solder and epoxy. Materials selection with respect to thermal resistance will be discussed. Finite Element and reliability software will be discussed to insure the design will perform to specification. Quality and reliability issues related to RF packaging and their present and future solutions will be outlined.

Who Should Attend? It will help the attendees to understand the application and assembly of RF and Microwave microelectronic package technology on the next level interconnect and the service environment that microelectronic packages must protect its components. Personnel (Design engineers and process engineers) entering the RF microelectronic packaging field will have a critical look at the electrical design, physical design, layout quality, reliability and material issues related to the development and manufacture of microwave modules. Non-technical personnel will learn the material and manufacturing intricacies of RF and Microwave microelectronic packages and the associated buzzwords used to describe them.

Tom Terlizzi *is VP at GM Systems, a Management and Technology consulting firm, providing Microelectronic Business & Technology plans, , Marketing & Sales strategy, Product development for microelectronic projects and business proposal support. He has designed and developed Power management systems, Single board computers, microelectronic circuits, hybrids, COB modules, ICs, RF modules, for over 30 years for military, aerospace, telecom and consumer markets as a VP/GM, Director of marketing, Chief Engineer, Operations/Engineering manager at Aeroflex, Norden/UTC, G.I. Microelectronics and Grumman. He spearheaded acquisitions of several high tech companies,ISO9000/Mil-PRF-38534 quality certifications. He received a BEE from CCNY, a MSEE from NYU-Poly & has published several articles, papers and tutorials at international conferences, edited books on electronic packaging, consulted for the DoD on advanced RF electronic packaging. Tom was the Metro ISHM Chapter President in 1983 and in his free time also writes a Blog for EDN Magazine Online - Looking @ electronics.*

M3: Introduction to Microelectronics Packaging
PDC Instructor: Thomas J Green, TJ Green Associates LLC

$600 (on/before 9/12/2014); $700 (after 9/12/2014)

Course Description: The instructor begins by broadly describing packaging terminology and reviews the alphabet soup of acronyms used throughout the electronics industry; terms such as: DIP, LCC, QFN, Hybrids, BGA, CSP, Flip Chip, 3D, TSV, WLP etc. The technology is then broken down by industry segments, beginning with high volume commercial packaging technology used in cell phones, tablets and handheld wireless devices, automotive, telecom and then progressing onto specialized packaging for low volume complex devices used in military/space/medical products as well as, RF microwave circuits, optoelectronics, LEDs and next generation packaging of MEMS and sensors. Lots of pictures, short video clips and pass around samples, along with simple explanations will help the attendee understand the technology drivers and key aspects of microelectronic packaging technology in a fun and interactive way. Besides a good overview the student will understand the basics of how to assemble and package single and multi-chip microcircuits, with a focus on the materials and processes and the associated equipment sets needed to support the industry. Wafer processes, probing and dicing, substrate selection, interposers, die attach using solders and epoxy, AU/Al/Cu wirebond processes, underfills, encapsulations, dam and fill, glob tops, transfer molding and hermetic packaging are all be reviewed with an eye on the important technical issues and industry drivers. Current hot topics and future industry trends will finish out the day and there will be plenty of time for questions.

Who Should Attend? This overview course is intended for those unfamiliar with microelectronics packaging technology. People in sales, purchasing, program management, new engineers, managers, equipment/material suppliers, people new to this industry or anyone looking to get a broad industry overview and review of the industry drivers, history and future trends are welcome to attend.

Thomas Green *is the principle at TJ Green Associates LLC (www.tjgreenllc.com) a veteran owned small business focused on training and consulting for military, space and medical microelectronic devices. He teaches a variety of public courses around the globe and in plant at major corporations and consults for a variety of medical device companies. He has thirty two years of experience in microelectronics working at positions in industry, academia and government. Tom has demonstrated expertise in die attach, wirebond, visual inspection, hermetic seal and leak testing processes. He has gained valuable experience over the past ten years in packaging and testing of devices for use as Class III medical implants and is often called on as an expert witness for hermeticity related failures. Tom is an active IMAPS member and Society Fellow. He has a B.S. in Materials Engineering from Lehigh University and a Masters from the University of Utah.*

M4: Polymer Challenges in Electronic Packaging Including 2.5D and 3D Integration
PDC Instructor: Jeffrey Gotro, InnoCentrix, LLC

$600 (on/before 9/12/2014); $700 (after 9/12/2014)

Course Description: The course will provide an overview of polymers and the important structure-property-process-performance relationships for electronic packaging. The main learning objectives will be: 1) learn how polymers are used in electronic packaging including die attach adhesives, underfills, mold compounds and substrate materials, 2) gain insights on how polymers are used in 2.5D and 3D packaging, 3) learn the key polymer challenges and processes for 2.5D and 3D packaging, 4) learn how to use polymer testing methods to gain insight into the key material properties relevant to electronic packaging, and 5) develop a foundation in rheology and rheological issues in electronic packaging. Participants are invited to bring problems for discussion.

Who Should Attend? Packaging engineers involved in the development, production, and reliability testing of electronic packages would benefit. Those interested in gaining a basic understanding of the role of polymers and polymer-based materials used in electronic packaging will also find this PDC valuable.

Dr. Jeff Gotro *has over thirty years' experience in polymers for electronic applications and composites having held scientific and leadership positions at IBM, AlliedSignal, Honeywell, and Ablestik Laboratories. Jeff is an expert in thermosetting polymers used in electronic packaging and has received invitations to speak at prestigious Gordon Research Conferences (Thermosetting Polymers and Composites). He has presented numerous invited lectures and short courses at technical meetings, has over 60 technical publications and 21 patents/patent applications. Jeff was an Adjunct Professor at Syracuse University in the Dept. of Chemical Engineering and Materials Science from 1986-1993. Jeff is a member of the Product Development and Management Association (PDMA), American Chemical Society (ACS), the Institute for Management Consultants (IMC), the Forensic Expert Witness Association (FEWA), and the International Microelectronics Assembly and Packaging Society (IMAPS).*

M5: Technology of Screen Printing
PDC Instructors: Art Dobie, Sefar Inc.; David Malanga, Heraeus, Inc., Thick Film Division
$600 (on/before 9/12/2014); $700 (after 9/12/2014)

Course Description: Screen printing continues to offer innovative and cost effective solutions to the increasing demands for higher circuit densities. This course is intended to increase the understanding of the screen printing process, thereby improving production yield and print quality.

Presented are some of the latest advancements in composition, screens, and printing technology that enable screen printing to meet future circuit density requirements as well as the definition required for microwave circuitry. The advantages of screen printing, an additive deposition process, are described and compared to alternative more costly and "less-green" subtractive deposition technologies. This course is applications-oriented in terms of how to optimize the screen printing process; how to use and specify screen correctly; rheology properties that affect print results; minimizing printing defects and trouble-shooting problems related to screens, inks and the printing process itself.

Who Should Attend? This course is targeted for production and process engineers, plant and production managers, supervisors, and all others interested in learning how to optimize and increase the use of the screen printing process.

Art Dobie *is Technical Marketing Manager for Sefar, Inc. He has been with Sefar 33 years since receiving his BS in Screen Printing Technology in 1980 from California University of Pennsylvania. Art has co-instructed the IMAPS "Technology of Screen Printing" PDC since its inception in 1991. He has delivered numerous technical presentations to screen-printing professionals at local, national and international level symposia. Mr. Dobie is a Life Member and Fellow of the Society of IMAPS, and received the 2006 IMAPS Technical Achievement Award for outstanding technical contributions to screen printing technology relating to microelectronics. In 1998, Art Dobie was inducted into the SGIA's Academy of Screen Printing Technology and is a co-recipient of the SGIA's 2010 David Swormstedt, Sr. Memorial Award.*

David Malanga *is currently Business Unit Manager Americas at Heraeus Precious Metals North America LLC, Thick Film Materials Division in West Conshohocken, PA.. David has over 20 years of experience at Heraeus working in R&D, formulating thick film and LTCC materials, Technical Service solving processing and application problems directly with customers, and as manager of the Sales Department. David has a B.S. and M.S. in Ceramic Science and Engineering from Rutgers University. David has published various articles on thick film resistors, conductors, LTCC materials, and component metallizations worldwide. He is a Life member and Fellow of the Society of IMAPS and has held both local and national positions in the organization.*

M6: Wire Bonding
PDC Instructor: Lee Levine, Process Solutions Consulting, Inc.
$600 (on/before 9/12/2014); $700 (after 9/12/2014)

Course Description: Wire Bonding is a welding process that is the dominant chip interconnection method. More than 15 trillion wires are bonded annually. The majority use gold wire, however, copper wire is experiencing rapid growth in market share. Copper provides benefits in cost, improved conductivity and stiffness. However, it is significantly harder than gold and achieving a robust, reliable process is a challenge. Gold, with defect rates in high-volume lead-frame applications below 10ppm, presents a significant barrier to entry but copper is meeting the challenge. Today more than 1 billion smart phones are produced, each having at least one stacked die package. Stacked dies are used to produce Systems In Package (SIPs) that enable the advanced features consumers demand.

The flexibility, reliability and yield of wire bonding make it a process worthy of careful study. Today's wire bonding equipment is capable of producing 24 wires/second (48 welds) with bond placement accuracy of Â±2.0Âµm. During the descent of the tool the bond head has an acceleration of >300g. Achieving highly repeatable bonds with the stated bond placement accuracy and yet accelerating at 300g requires exceptional engineering design. The wire bonder is one of the worlds most advanced machines requiring high speed pattern recognition, ultra-light, stiff sub-assemblies (imagine trying to achieve the same speed and accuracy with a graphite fishing rod), and feed forward control systems. The course will cover:

Introduction
- A snapshot of some microelectronic packages
- Size of the market
- Cost of a wire bond
- Ultrasonic Welding
- Intermetallics
- Bond Testing

- Copper wire bonding
- Looping and Ball Formation
- Wire
- Fine Pitch Bonding
- Plating
- Wire Bond variations (ball bumping)

Who Should Attend? Engineers in R&D, QA, QC, manufacturing, process development, and advanced technicians. It is assumed that participants have some familiarity with wire bonding and general device assembly technologies.

Lee Levine *is a consultant for Process Solutions Consulting, Inc. where he provides process engineering consultation, SEM/EDS analysis, and wire bond training. Lee's previous experience includes 20 years as Principal and Staff Metallurgical Process Engineer at Kulicke & Soffa and Distinguished Member of the Technical Staff at Agere Systems. He has been awarded 4 patents, published more than 70 technical papers, and in 1999 won the John A. Wagnon Technical Achievement award from the International Microelectronics and Packaging Society (IMAPs). Major innovations include copper ball bonding, loop shapes for thin, small outline packages (TSOP and TSSOP, and CSPs) and introduction of DOE and statistical techniques for understanding semiconductor assembly processes. He is an IMAPs Fellow and a senior member of IEEE. He is a Contributing Editor for TAP Times, an online packaging newsletter. Lee is a graduate of Lehigh University, Bethlehem, Pa where he earned a degree in Metallurgy and Materials Engineering.*

MONDAY MORNING HALF-DAY PDCs: (10am-1:45pm)

- ENIG - Electroless Nickel & Immersion Gold Plating for Electronics: From the Plating Solutions to the Equipment;
- High-Temperature Electronics;
- MEMS and nanoMEMS Devices and Applications;
- Package level integration : 2-d, 2.5-d and 3-d, impact on Mobile Systems

MA1: ENIG - Electroless Nickel & Immersion Gold Plating for Electronics: From the Plating Solutions to the Equipment

PDC Instructor: Fred Mueller, General Magnaplate Corp.

$400 (on/before 9/12/2014); $500 (after 9/12/2014)

Course Description: Provide a thorough overview of the use of electroless nickel and immersion gold and other precious metals used for a variety of applications in the field of electronics; Review the engineering differences and troubleshooting problems associated with the ENIG plating process; Presents methods for controlling the properties of plating solutions to maximize the deposits properties, including Laboratory Controls Electroless Nickel/Immersion Gold, Solderability and Solder Joint Reliability as Functions of Process Control - What lack of ENIG process controls can result in black pad?

Who Should Attend? This course is intended as an introductory to intermediate level course for process engineers, quality engineers, and managers responsible for Plating for Electronics.

Fred Mueller *is a consultant and serves as a national certified instructor for the American Electroplaters and Surface Finishing Society (AESF). He has over twenty-five years of experience in the plating industry in printed circuits and plating for electronics. He is currently the National Quality Manager at General Magnaplate, Linden, NJ. As a Chemist, Fred has conducted experiments and presented technical papers at SurFin on various topics in electroplating. He is very active in the AESF Foundation currently serving as Vice President on the National Board.*

MA2: High-Temperature Electronics
PDC Instructor: Randall Kirschman, Consultant
$400 (on/before 9/12/2014); $500 (after 9/12/2014)

Course Description: High-Temperature Electronics is a valuable option for improving overall system performance: increased efficiency, decreased size and weight, simplified maintenance and improved reliability.

The focus of this course is semiconductor electronics at high temperatures: device behavior, applications, advantages and drawbacks, technical issues, and present situation. Basic materials characteristics related to electronics at high temperatures, and passive electronic component behavior, are included. The temperature range covered in this course extends from +125C upward, as high as 1000C. Depending on the temperature range, HTE semiconductor devices may be based on Si, SiGe, GaAs, SiC, GaN, C (diamond) and other materials.

Course Objectives: Provide an overview of situations where the technologies of electronics and high temperatures are brought together. Provide an overview of the applications for high temperature electronics. Survey the relationships between fundamental phenomena, materials behavior, and device and system characteristics and performance at high temperatures. Overview the behavior of materials and components used in electronics at high temperatures: metals, ceramics, plastics, passive components, semiconductor materials and devices, and electronic circuits and assemblies. Provide practical information on materials, devices, circuits and techniques for those involved in high-temperature electronics.

Who Should Attend? Engineers and technical persons involved in developing electronics for high temperatures; also project managers and students who want an introduction and overview of the subject.

Dr. Randall Kirschman *is an internationally recognized authority on extreme-temperature electronics. He has been consulting to industry, government and academe since 1980 on microelectronic materials and fabrication technology, and electronics for extreme temperatures. Before going into business for himself, he managed the processing laboratory at the R&D Center at a division of Eaton Corporation, where he was responsible for the fabrication of thin-film hybrids. Before that, he was a staff member of the Jet Propulsion Laboratory, performing research on semiconductor materials and devices. During 1990-91 he was a Visiting Senior Research Fellow at the Institute of Cryogenics, University of Southampton, England. Between 1998-2005, he was a member of the Physics Department at Oxford University. He edited the 1999 IEEE Press/Wiley book High-Temperature Electronics. He completed his undergraduate studies at the University of California, and earned his Ph.D. in Physics and Electrical Engineering at the California Institute of Technology in 1972.*

MA3: MEMS and nanoMEMS Devices and Applications
PDC Instructor: Slobodan Petrovic, Oregon Institute of Technology

$400 (on/before 9/12/2014); $500 (after 9/12/2014)

Course Description: This full day course will explore futuristic concepts that combine MEMS and nanoscience. The merging of nanoscience and microelectromechanical systems presents an opportunity for development of next generation technologies for use in computers, wireless communication, biomedicine, and a variety of sensors.

The course will start by providing an overview of the MEMS principles of operation, fabrication methods, and in particular the materials used in building MEMS structures. Variety of MEMS devices will be discussed while a particular emphasis will be placed on MEMS in wireless communication; and sensors and actuators used in industrial, medical, and automotive applications.

The introduction to nanoscience will start by evaluating how size can influence the properties of nanoscale systems. The nanomaterial synthesis and characterization methods will be explored next. The highly speculative discussion will offer a possibility for using nanoscale phenomena for technological purposes related to MEMS. The emphasis will be placed on merging the nanoscience with MEMS fabrication principles, design considerations, integration aspects, and packaging.

In the third section, the integration of power supplies and energy storage devices with MEMS and nanoMEMS devices will be discussed. These devices will be the key in the packaging and for autonomous function of future devices. The general concept of nanoscience for energy will be discussed, in particular nanoscale batteries, fuel cells, hydrogen production, solar cells, and biological materials for energy production.

Who Should Attend? The course is open to anyone with general understanding of the physics, chemistry, and material science. The participants will have the opportunity to explore highly speculative, futuristic concepts and develop visionary views of the technological possibilities. The course is open to participants with no prior MEMS, nantotechnology, or power sources knowledge and would provide a reasonably broad general introduction into all three areas of technology.

Dr. Slobodan Petrovic *is an associate professor at the Oregon Institute of Technology in Portland, OR. His research interests are in the areas of MEMS fuel cells, sensor media compatibility, hydrogen generation and storage, and dye-sensitized solar cells. Prior to that, he was at the Arizona State University, where he taught courses in MEMS, Sensors, and alternative energy. Dr. Petrovic also held appointments at Clear Edge Power as a Vice President of Engineering; at Neah Power Systems as Director of Systems Integration; and Motorola, Inc. as a Reliability Manager. Dr. Petrovic has over 25 years of experience in MEMS, sensors, energy systems; fuel cells and batteries; and electrochemical solar cells. He has over 50 journal publications and conference proceedings; 2 book contributions and 24 pending or issued patents.*

MA4: Package Level Integration: 2-D, 2.5-D and 3-D, Impact on Mobile Systems
PDC Instructor: Dev Gupta, APSTL

$400 (on/before 9/12/2014); $500 (after 9/12/2014)

Course Description: For the first time a course that combines electrical performance (bandwidth, power for data transfer) of various 2-D, 2.5-D and 3-D Packaging schemes for Processor - Memory combination with Process details / complexity & cost. So as to give a range of choices to the Package Designer. Review key features of several types of 3-D packaging: using TSVs, more traditional vertical interconnects, comparison. Roadmap for Processor - Memory in Mobile systems like Smart Phones & Tablets. Physical and electrical attributes, Packaging trends, Future options.

Who Should Attend? Package Designers, Process Developers, Managers, Analysts.

Dr. Dev Gupta *has 25 years of experience in pioneering Advanced Packaging technologies like various types of Flip Chip that have now become industry standards. He specializes in applying theoretical methods to identify new applications and speedy process development. At Motorola in the early '90s he developed electroplated solder bump technology, assembly robots & processes, micro-pillar bumps, integrated microwave passives that all went into products like ASICs, uProcessrs & Mobile Phones. At Intel his Team developed the Organic Substrate technology and its High Volume Manufacturing that led to its wide adoption. At APSTL he is now developing new Packages for Mobile Phones with high Power Efficiency. Dr. Gupta has frequently offered short courses at IEEE, SemiCon and IMAPS Conferences.*

MONDAY AFTERNOON HALF-DAY PDCs: (2:15pm-6pm)

- Low-Temperature Electronics;
- Package on Package Technology - What It Is, What Works, What Doesn't Work;
- Thermal And Mechanical Simulation Techniques For IC Package Yield, Reliability And Performance

MP1: Low-Temperature Electronics
PDC Instructor: Randall Kirschman, Consultant
$400 (on/before 9/12/2014); $500 (after 9/12/2014)

Course Description: Low-Temperature Electronics (LTE) is a valuable option when ultimate performance is needed from devices, circuits, and systems. Temperature may be thought of as an additional design choice when justified by system performance requirements.

Applications include microwave receivers for cell phone base stations, radio astronomy, and deep-space communication; signal-conditioning circuits for low-temperature infrared sensors; tracking systems for cryopreservation of biological specimens, supercomputers in which critical subsystems are cooled by liquid nitrogen. Benefits from cooling include faster switching, higher efficiency, lower noise and higher sensitivity. At the same time there are technical and non-technical challenges.

The focus of this course is semiconductor (rather than superconductor) electronics at low temperatures: applications, materials and techniques, advantages and drawbacks, technical issues and present situation. Topics include semiconductor device behavior and capabilities, packaging and assembly materials characteristics as a function of temperature, passive electronic component behavior, and reliability issues, as well as practical aspects of choosing components, packaging and assembly materials and techniques. The temperature range covered extends from room temperature down to absolute zero (â□"273oC), with emphasis on the cryogenic range, approximately â€150oC and below.

Course notes include approximately 150 slides, approximately 120 pages of supplementary notes, plus more than 1000 references/ bibliographic items.

Who Should Attend? Engineers and technical persons in research or development of electronics for low-temperature applications. Anyone considering use of low temperatures in future hardware designs. Familiarity with electronic devices and circuits is an advantage; however, materials and device fundamentals will be reviewed.

Dr. Randall Kirschman *is an internationally recognized authority on extreme-temperature electronics. He has been consulting to industry, government and academe since 1980 on microelectronic materials and fabrication technology, and electronics for extreme temperatures. Before going into business for himself, he managed the processing laboratory at the R&D Center at a division of Eaton Corporation, where he was responsible for the fabrication of thin-film hybrids. Before that, he was a staff member of the Jet Propulsion Laboratory, performing research on semiconductor materials and devices. During 1990-91 he was a Visiting Senior Research Fellow at the Institute of Cryogenics, University of Southampton, England. Between 1998-2005, he was a member of the Physics Department at Oxford University. He edited the 1999 IEEE Press/Wiley book High-Temperature Electronics. He completed his undergraduate studies at the University of California, and earned his Ph.D. in Physics and Electrical Engineering at the California Institute of Technology in 1972.*

MP2: Package on Package Technology - What It Is, What Works, What Doesn't Work
PDC Instructor: Ning-Cheng Lee, Indium Corporation

$400 (on/before 9/12/2014); $500 (after 9/12/2014)

Course Description: This course covers Package on Package (PoP) Technology, including trends, designs, material selection, processes, and reliability. The approaches of enhancing the reliability will be discussed in details, including effect of fluxes, solder alloy types, processes, profiles, via designs, and ball sizes. Being the solution with the highest potential, epoxy flux will be introduced and will be compared with other solutions. Finally, head in pillow control at reflow soldering, particularly at PoP will be instructed. The control includes considerations on materials, processes, and designs.

Course Content:

1. Trends
2. Designs
3. Processes
    - 3-1.General Processes.
    - 3-2. Rework of PoP.
    - 3-3. Processes - Selection of Dip Transfer Fluxes and Solder Pastes for PoP Assembly
    - 3-4. Processes - Low Volume PoP Assembly Process Development
    - 3-5. Processes - Design for Efficient PoP Underfilling
    - 3-6. Processes - Comparison of Various Polymeric Reinforcement Approaches for PoP/CSP
4. Reliability - One-Pass vs Two-Pass
5. Reliability - Effect of SOP & Material on Yield & Drop Test Performance
6. Reliability - Effect of Materials & Profiles
7. Reliability - Materials Selection & Parameter Optimization
8. Reliability - Mixed Alloy
9. Reliability - Effect of Coplanarity and Design
10. Reliability - Effect of Ball Size, Via Size, Alloy Type on Stack-up Height & Reliability
11. Reliability - Opens/Head-in-Pillow - The Primary Failure Mode of PoP

Who Should Attend? Anyone who cares about successful implementation of package on package technology, and like to know how to achieve it should take this course.

Dr. Ning-Cheng Lee *is the Vice President of Technology of Indium Corporation of America. He has been with Indium since 1986. Prior to joining Indium, he was with Morton Chemical and SCM. He has more than 20 years of experience in the development of fluxes and solder pastes for SMT industries, plus experience in underfills and adhesives. He received his PhD in polymer science from University of Akron in 1981, and BS in chemistry from National Taiwan University in 1973. Ning-Cheng is the author of "Reflow Soldering Processes and Troubleshooting: SMT, BGA, CSP, and Flip Chip Technologies", and co-author of "Electronics Manufacturing with Lead-Free, Halogen-Free, and Conductive-Adhesive Materials". He was honored as 2002 Member of Distinction from SMTA, 2003 Lead Free Co-Operation Award from Soldertec, 2006 Exceptional Technical Achievement Award from CPMT, 2007 Distinguished Lecturer from CPMT, 2009 Distinguished Author from SMTA, and 2010 Electronics Manufacturing Technology Award from CPMT.*

MP3: Thermal and Mechanical Simulation Techniques for IC Package Yield, Reliability and Performance

PDC Instructor: Kamal Karimanal, Cielution LLC

$400 (on/before 9/12/2014); $500 (after 9/12/2014)

Course Description: The industry is becoming increasingly aware of the fact that thermal and mechanical factors related to packaging and assembly are crucial hurdles to the enablement of next generation IC and photonic products. These challenges are pervasively felt at all stages of the product development cycle starting from Layout, IC design, power management, assembly processing strategy, package design, and testing. Due to the need to narrow down from a myriad of costly choices even prior to test chip or prototype development, engineering simulation is an important tool at the disposal of the engineer. As a result, engineers from all IC design and packaging background are interested in utilizing thermal and mechanical simulation.

This is an introductory course on thermal and mechanical simulation techniques pertaining to assembly and packaging designed for engineering professionals involved in the enablement of monolithic IC products as well as TSV based 3D stacked SOCs. Following are the course contents:

- Direct Thermal Modeling Techniques: Steady-State, Transient, tips for non-thermal engineer.
- Compact Thermal Modeling: Applicability of traditional CTM, Novel CTM techniques.
- Overview of mechanical challenges to packaging and assembly: warpage, assembly Yield, CPI effects on Yield & reliability
- Wafer warpage estimation: applicability of Stoney formula, simulation and measurement techniques
- Assembly process modeling techniques: CTE, Reference temperature, Element Birth & Death.
- The concept of Global/Local Modeling: Lumped modeling techniques.
- Mechanical Risk Indicators: Warpage, Stress, Stress Intensity Factors and Energy Release rate.
- Chip level mobility/stress distribution: Contributions from package, TSV and devices.

Who Should Attend? Any Engineering professional involved in the enablement of next generation IC and SOC products with interest in the Thermal and mechanical challenges.

Dr. Kamal Karimanal *is the Founder of Cielution LLC, which is an Engineering simulation software and services company serving the electronics supply chain. Dr. Karimanal has served in several engineering simulation focused roles at IERC, Fluent Inc., ANSYS Inc., Globalfoundries, and Juniper Networks. Dr. Karimanal has contributed to several detailed and compact modeling methodologies which are being widely used by the electronics industry today. He has written several conference and journal papers and online application notes. Dr. Karimanal received his Ph. D in Mechanical Engineering from The University of Texas at Austin.*

Thursday, October 16, 2014

All Thursday PDCs are Half-Day Courses (4-hours): 8:00 am - 12:00 pm
10:15 AM - 10:30 AM: Coffee Break in Foyer

T1: Chip Packaging Processes and Materials
PDC Instructor: Syed Sajid Ahmad, North Dakota State University/CNSE
$400 (on/before 9/12/2014); $500 (after 9/12/2014)

Course Description: Myriad of package types require the use of some common and uncommon processes and materials for their manufacture. The course will provide an overview of prevalent processes and materials for conventional and advanced packaging and review their impact on the integrity of finished products. Course will also discuss the quality and reliability metrics, testing methods, failure modes and their resolution.

Who Should Attend? Designers will learn about the assembly processes and their relation to design. Engineers will learn about processes outside their area of expertise. Non-engineering personnel will get introduced to the chip assembly world.

Syed Sajid Ahmad *contributed to quality and reliability enhancement of assembly processes at Intel (1979-89), especially wire bond. Ahmad also contributed to packaging development at National Semiconductor (1990) and managed quality at GigaBit/ TriQuint (1990-91). His major work at Micron Technology (1991-2003) involved the development and implementation of advanced packaging. At the Center for Nanoscale Science and Engineering, Ahmad's focus is on enhancing research and manufacturing capabilities at the center in the areas of thin film, thick film, chip scale packaging (CSP) and surface mount technology (SMT). Ahmad has 35 international publications and presentations and holds 54 patents.*

T2: Fundamentals of Microelectronics Packaging
PDC Instructor: John Pan, Cal Poly State University
$400 (on/before 9/12/2014); $500 (after 9/12/2014)

Course Description: The objective of this course is to introduce materials, processes, and reliability of microelectronics and electronic packaging. Course outline:

Introduction to Microelectronics Packaging
- Electronics Packaging Hierarchy and Functions
- Electronics Package Types
- Electronics Packaging Trends

Microelectronics Packaging Materials and Processes
- Die attachment
- Wire bonding
- Flip Chip
- Encapsulation and Sealing

Organic PCB Materials & Processes
- PCB Materials
- Multi-layer PCB Fabrication Processes
- High-density Interconnection

Electronics Assembly Processes
- Surface Mount Assembly (stencil printing, pick and place, and solder reflow)
- Soldering Basic (solder and solder paste, soldering wetting, solder phase diagrams, and soldering mechanism)
- Reflow soldering and wave soldering
- Lead-free solder joint reliability

Ceramics Substrate Materials & Processes

- Ceramics Materials
- LTCC
- HTCC

At the end of this course, participants should be able to:

- Describe materials and fabrication processes of multi-layer printed circuit boards and high-density interconnections.
- Describe PCB assembly processes and soldering.
- Describe microelectronics and electronic packaging processes including die attachment, wire bonding, flip chip, and encapsulation.
- Evaluate different packaging substrate materials such as organic, ceramic, LTCC, and HTCC based on electrical, mechanical, and thermal performance as well as cost and reliability.

Who Should Attend? This course is designed for engineers and scientists in R&D, process/product development, and manufacturing who have little knowledge or want to broaden knowledge in materials and processes of microelectronics and electronic packaging.

Dr. John Pan *is a professor in Industrial and Manufacturing Engineering Department at California Polytechnic State University, San Luis Obispo. His research interests include the materials, processes, and reliability of microelectronics packaging. He has authored or co-authored over 40 technical papers. He is a Fellow of IMAPS and a recipient of the 2011 IMAPS Outstanding Educator Award. He is currently the Editor-in-Chief of Journal of Microelectronics and Electronic Packaging and an Associate Editor of IEEE Transactions on Components, Packaging and Manufacturing Technology.*

T3: IC Fabrication and Electronic Packaging
PDC Instructor: Aicha Elshabini, University of Idaho

$400 (on/before 9/12/2014); $500 (after 9/12/2014)

Course Description: This course serves as an introduction to the fabrication of microelectronic devices. Topics include the basics of IC structures, clean room protocol, photolithography, film growth and deposition, as well as IC interconnect technologies. The second portion aims at 1) technical drives and trends including performance, low and effective cost, 2) reliability and yield issues in wirebonding and flip chip bonding originating from chip-to-package, 3) mechanical, metallurgical, chemical failure mechanisms, 4) electrical design and performance analysis, 5) thermal management issues, 6) rework, fluxing, and curing underfill, 7) known a good die, and 8) aspects of electronic packaging to impact the performance of housed electronic devices within the package.

Course Contents: Semiconductor Substrates, Hot Processing, Ion Implantation, Thermal Oxidation, Rapid Thermal Processing, Optical Lithography, Photoresists, Lithographic Techniques, Plasmas, Etching, Evaporation, Sputtering, Chemical Vapor Deposition, Epitaxial Growth, Device Isolation Contacts and Metallization, CMOS and Transistor Technologies. The second portion of the course aims at substrates (organic, metal, semiconductor, and ceramic) design and fabrication, surface mount technology (SMT), passive component integration, multichip modules (system in a package & 3D packaging), and first level assembly, clean room protocol, electrical, mechanical, and thermal design, simulation, and process considerations

Distinguished Professor Aicha Elshabini, Ph.D., *P.E., IEEE Fellow, IMAPS Fellow Academic Advisor of IMAPS, NSBE, and SWE. Elshabini graduated from Cairo University, Egypt, Communications and Electronics, B.Sc., ECE, 1968-1973, from Toledo University, Toledo, Ohio, Microelectronics, M.S.E.E., 1973-1975, and from Colorado University, Boulder, Colorado, Solid State Physics, Devices, and Optoelectronics, Ph. D., ECE, 1975-1978/1979.*

International Society for Hybrid Microelectronics (ISHM), Currently named IMAPS (International Microelectronics Assembly and Packaging Society, effective November 1996 since merging with IEPS), Fellow Member Elected (1993) for "Continuous Contribution to Microelectronics & Microelectronics Industries".IMAPS Publication Committee, Member 1990-2001, and Chair, 2001-2005. Founding Editor of the International Journal of Microcircuits and Electronic Packaging, IMAPS, 1991-2001.Academic Advisor for IMAPS, NSBE, and SWE (Society for Women Engineers).Elshabini was awarded the 1996 John A. Wagnon Technical Achievements Award from IMAPS. She was awarded the 2006 Daniel C. Hughes Memorial Award from IMAPS, and in 2007, the Outstanding Educator Award. With this third award from IMAPS Dr. Elshabini became the first woman to earn three top awards from IMAPS in its 40 year history.

T4: Interposers - Silicon, Organic and Glass
PDC Instructor: Venky Sundaram, Georgia Tech PRC
$400 (on/before 9/12/2014); $500 (after 9/12/2014)

Course Description: This course provides the most comprehensive summary of interposer technologies, market drivers, application examples and infrastructure evolution, covering silicon, organic and glass interposers. Interposers bridge the interconnect gap between back end of the line (BEOL)pitch and current organic BGA packages. Interposers started out as a 2.5D multi-die integration step towards full 3D IC stacking. However, they are now viewed as a system integration platform with pervasive applications in smart mobile, cloud computing and networking, photonics, analog/power, MEMS, sensors, RF/mm-wave, medical electronics and many other applications. In the past couple of years, the technology development and manufacturing infrastructure maturity has been progressing rapidly. This year's PDC by one of the top interposer experts in the world, includes significant new material covering the latest advances in 2.5D and 3D interposers. The course will address both fundamentals of interposer technology, as well as applications and supply chain infrastructure. An extensive review of three major interposer options being pursued, namely, silicon, organic and glass, will be provided. The course will be interactive and include audience Q&A and samples of latest interposer demonstrators will be passed around for a hands-on experience.

Who Should Attend? This is a must attend course for anyone interested in state-of-the-art interposer technologies. The course is especially valuable to semiconductor, electronics systems, and packaging industry personnel in engineering, management, corporate technology strategy, pathfinding and marketing teams.

Dr. Venky Sundaram *is a Research Professor and manages the Industry Research Programs at the 3D Systems Packaging Research Center (PRC), Georgia Tech. He is the Program Director for the largest Low Cost Glass Interposer & Package (LGIP) industry consortium with more than 30 active global industry members. He is a globally recognized expert in 3D systems packaging, and has pioneered major technologies including embedded RF passives in organic substrates, chip-last die embedding and glass interposers. His research expertise is in the areas of System on a Package (SOP) technology, 3D packaging and integration, ultra-high density interposers, embedded components, bio-medical device packaging, LED packaging and systems integration research. He has mentored more than 15 PhD and MS students, and teaches a laboratory course every Fall on SOP Substrates, ECE/MSE 4755. He is a co-founder of Jacket Micro Devices, an RF/wireless start-up acquired by AVX. Dr. Sundaram has served as session chair at major global packaging conferences, serves on the Advanced Packaging Committee of SEMI, is the co-chairman of the IEEE CPMT Technical Committee on High Density Substrates, serves on the Editorial Advisory Board of Chip Scale Review magazine, and is in the Executive Council of IMAPS as Director of Education Programs. Dr. Sundaram has won several best paper awards and has 15+ patents and 150+ publications. He received his BS from IIT Mumbai, and MS and PhD in Materials Science and Engineering from Georgia Tech.*

T5: Packaging and Testing of Implanted Medical Devices
PDC Instructor: Thomas J Green, TJ Green Associates LLC
$400 (on/before 9/12/2014); $500 (after 9/12/2014)

Course Description: Hermetic and non-hermetic packaging and testing of microelectronics, sensors, MEMS, hybrids and microwave components for use as implanted Class II/III devices in vivo is of critical importance. Cost, reliability, small form factors, biocompatibility and patient safety are driving concerns. This course begins with an overview of traditional hermetic packaging and testing approaches that have been in use for over forty years. Most pacemakers, IPGs, cochlear implants in use today follow a prescribed and proven path of hermetic sealing and testing to assure product reliability and patient safety, which includes hermeticity testing in accordance with MIL-STD-883 Test Method 1014.

Today however, the research is directed at development of a non-hermetic package that is at least as good as the proven path. Packages made from polymeric materials require a different approach from a manufacturing and testing standpoint. The problem is now one of moisture diffusion through the barrier and package interfaces. Candidate materials such as parylene, PDMS, various ALD and CVD organic and inorganic coatings, LCP, silicones etc. are reviewed and application processes discussed. How to test and evaluate.

Who Should Attend? This course is intended as an introductory to intermediate level course for process engineers, designers, quality engineers, and managers responsible for package seal, hermeticity testing and for those responsible for evaluating non-hermetic packages.

Thomas Green *is the principle at TJ Green Associates LLC (www.tjgreenllc.com) a veteran owned small business focused on training and consulting for military, space and medical microelectronic devices. He teaches a variety of public courses around the globe and in plant at major corporations and consults for a variety of medical device companies. He has thirty two years of experience in microelectronics working at positions in industry, academia and government. Tom has demonstrated expertise in die attach, wirebond, visual inspection, hermetic seal and leak testing processes. He has gained valuable experience over the past ten years in packaging and testing of devices for use as Class III medical implants and is often called on as an expert witness for hermeticity related failures. Tom is an active IMAPS member and Society Fellow. He has a B.S. in Materials Engineering from Lehigh University and a Masters from the University of Utah.*

T6: Understanding the Common Failure Modes from a Physics of Failure Perspective
PDC Instructor: Greg Caswell, DfR Solutions
$400 (on/before 9/12/2014); $500 (after 9/12/2014)

Course Description: There are numerous failure modes and mechanisms that can impact a product. Understanding how they occur and how to obviate them during the design stage can vastly improve a product's ability to withstand the rigors of its intended environment.

This course will address the common failure modes associated with printed circuit boards, passive components, Integrated Circuits, High Brightness LEDs, QFNs, CSPs, PoP, and MEMs along with the effects of long term storage of components.

Physics of Failure (PoF) is a proactive science based philosophy that addresses material science, physics and chemistry and provides the basis for the student to develop an up-front understanding of failure modes/mechanisms. Knowing how things fail is equally important to understanding how and why things work by enabling engineers and designers to be knowledgeable about root causes of failures so that they can be designed out in new products.

PoF provides a scientific basis for evaluating usage life and hazard risks for new materials, structures and technologies when exposed to their actual operating conditions.

Examples of each failure mode/mechanism will be illustrated along with insight into methods for obviating them.

Who Should Attend? Engineers or managers who would like to have a better understanding of Physics of Failure and the types of issues that can be encountered in circuit boards, passive components, ICs, LEDs, PoP packaging, MEMs, as well as the issues associated with solder wearout, long term storage reliability, tin whiskers, etc.

Greg Caswell *is widely recognized as a pioneer in surface mount technology (SMT) and has 42 years of experience in the electronics industry. In his current position he is a Sr. Member of the Technical Staff for DfR Solutions. Greg has been involved with IMAPS in numerous capacities: 1984 Centex Chapter President, 1986 ISHM Vice President, 2001 President of the IMAPS, 1989-2000 ATW Chairman, 2008 GBC Chair, 2007 General chair for Symposium, and 2009-2012 Editor Advancing Microelectronics. He has received the IMAPS Technical Achievement (1986), Fellow of the Society (1993), and Daniel C Hughes Memorial Award (1995). He received his Bachelor of Science in Electrical Engineering from Rutgers University and also has a Bachelors in Management from St. Edwards University in Austin.*

Register Online

PDC registration is listed under SESSIONS during the online registration process

Solders and Thermal Interface Materials

Gold-Based Solders

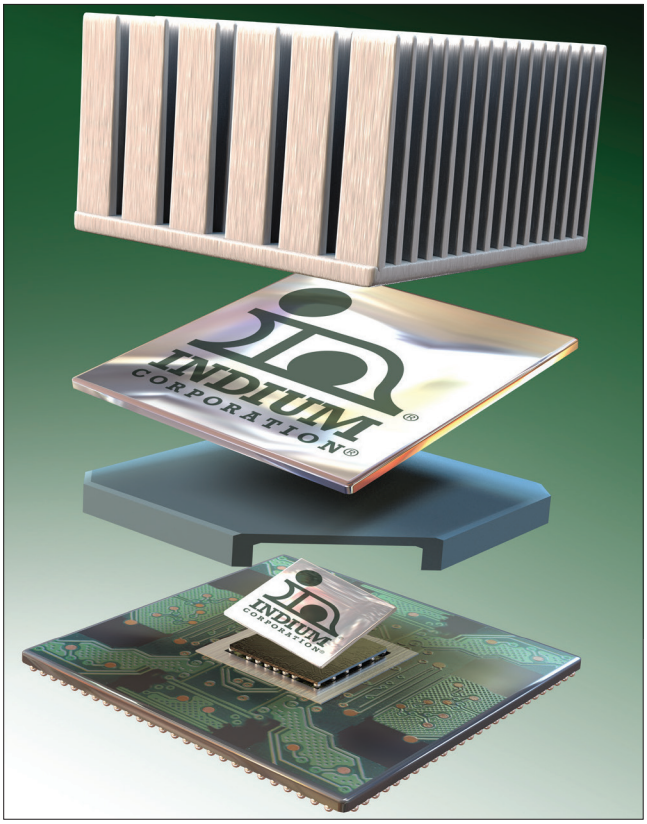
- Complex geometries, sizes, and flatness
- A variety of alloys for specific applications
- Extensive application knowledge

Metal TIMs

- Residue-free
- No pump out or bake out
- Thermal conductivity up to 86W/mK
- Available in tape & reel and tray packs

Flip-Chip Fluxes

- Eliminate joint-cracking
- Reduce cost caused by cleaning
- Ultralow residue eliminates underfill voiding and excessive epoxy bleedout
- Customer-proven compatibility with standard MUF and CUF



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Technical Program At-a-Glance

Tuesday, October 14, 2014 — 8:00 AM—11:15 AM

INTERPOSERS & 3D PACKAGING	MODELING, DESIGN, & TEST	MATERIALS & PROCESSES	ADVANCED PACKAGING INTERCONNECTS & ASSEMBLY	FUTURE OF PACKAGING	SPECIAL SESSIONS: 3D & EMBEDDING, AND RELIABILITY
TSV Materials & Processes *Chairs: Vidhya Ramachandran, Qualcomm; Sesh Ramaswami, Applied Materials*	**Design & Analysis for Reliability** *Chairs: Gopal Jha, Avago Technologies Inc.; John Pan, Cal Poly State University*	**Advanced Materials & Novel Assembly Processes** *Chairs: Allan Beikmohamadi, DuPont; Yasuhiro Kawase, Mitsubishi Chemicals*	**Flip Chip - Solder** *Chairs: Mary Cristina Ruales Ortega, El Sistema Universitario Ana G. Méndez; John Bolger, Department of Defense; Linlin Yang, Alta Devices*	**Future of Packaging** *Chairs: Erica Folk, Northrop Grumman; Nick Renaud-Bezot, AT&S AG*	**3D and Embedding** *Chairs: Doug Shelton, Canon USA, Inc.; Woong-Sun Lee, SK Hynix, Inc.*
2:00 PM—6:35 PM					
Interposers/3D Integration - I *Chairs: Urmi Ray, Qualcomm; Kyu-oh Lee, Intel Corporation*	**Modeling & Design for SI, PI and EMC** *Chairs: Ege Engin, San Diego State University; Gabriel Parès, CEA LETI*	**Polymers, Underfill, Encapsulants & Adhesives** *Chairs: Jeff Gotro, InnoCentrix; Lyndon Larson, Dow Corning*	**Wirebonding & Stud Bumping** *Chairs: Dan Evans, Palomar Technologies; Lee Levine, Process Solutions Consulting*	**Medical Device Packaging** *Chairs: Andre Rouzaud, CEA/Léti; Susie Johansson, Starkey Hearing*	**Reliability I** *Chairs: Aicha Elshabini, University of Idaho; Stevan Hunter, ON Semiconductor*

Wednesday, October 15, 2014 — 8:00 AM—11:15 AM

Glass Interposers *Chairs: Steve Annas, Triton MicroTech; Aric Shorey, Corning*	**Thermal and Thermo-Mechanical Modeling** *Chairs: Kamal Sikka, IBM Systems & Tech Group; Bill Marsh, Northrop Grumman ES*	**Substrate Materials and Technology** *Chairs: Michael Folk, Northrop Grumman; Anwar Mohammad, Flextronics; Kiran Vanam, Qualcomm*	**Electronic Packaging for Harsh Environment and Hi-Reliability (Mil/Aero)** *Chairs: Benson Chan, i3 Electronics, Inc.; Sergei Zotov, University of CA, Irvine*	**MEMS and Sensors Packaging** *Chairs: Matt Apanius, SMART Microsystems; Julie Adams, UBOTIC Company; Igor Prikhodko, Analog Devices*	**Reliability II** *Chairs: Martin Schneider-Ramelow, Fraunhofer IZM; Susan Bagen, Micro Systems Technologies, Inc.*
2:00 PM—5:30 PM					
Interposers/ 3D Integration - II *Chairs: John Hunt, ASE US Inc.; Tolga Tekin, Fraunhofer IZM*	**Testing Methods and Process** *Chairs: Akhlaq Rahman, Thin Film Technology Corporation; Jim Will, Honeywell*	**LTCC and Ceramic Substrate Technologies** *Chairs: Daniel Krueger, Honeywell; Ken Peterson, Sandia National Labs.*	**Novel Wafer Finish Processes** *Chairs: Ron Jensen, Honeywell; Rajiv Roy, Rudolph Technologies*	**Power Packaging** *Chairs: Mark Hoffmeyer, IBM; Doug Hopkins, North Carolina State University; Fred Barlow, University of Idaho*	

Thursday, October 16, 2014 — 1:00 PM—5:00 PM

Advanced Interconnect Innovations *Chairs: Jeffrey Hartman, Northrop Grumman; Josh Luff, Honeywell*	**RF, MM/Microwave Applications** *Chairs: Ken Kuang, Torrey Hills Tech; Hassan Hashemi, Newport Media*	**Bonding Materials and Processes** *Chairs: Maria Durham, Indium Corp.; Ganesh Krishnan, Formfactor Inc.; Li Jiang, Texas Instruments*	**Photonic Packaging** *Chairs: John Mazurowski, Penn State Electro-Optics Center; Vivek Raghunathan, Intel Corporation*	**Printed Electronics & Additive Manufacturing** *Chairs: Mike Newton, Newton Cyberfacturing; Samson Shahbazi, Heraeus Electronic Materials Division*	

Keynotes and Panel Discussion

Tuesday, October 14, 2014 • 12:00 PM - 12:45 PM

Classical Packaging - Its Strengths and Limitations

Wednesday, October 15, 2014 • 11:30 AM – 12:15 PM

High-end Packaging Development: Opportunities and not Challenges

Thursday, October 16, 2014 • 8:00 AM - 12:00PM

Future of Packaging Keynotes & Panel Discussion

Technical Program

Welcome Reception | 6:00 PM - 8:00 PM

Poolside at the Town & Country, San Diego, CA

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Featuring Natel's Second Annual Supplier of the Year Awards…

Based on the success of last year's awards, NATEL EMS will again recognize its best supplier's Monday evening with its Natel supplier of the Year awards during IMAPS 47th annual International Symposium. The awards presentation will be held at the Town Country Resort and Conference Center in San Diego, CA during the Welcome Reception, Monday, October 13, 2014. "The Supplier of the Year award winners represent a partnership, dedication and commitment to consistently perform above expectations. This continues to play an important role in Natel's success," said Sudesh Arora, President of Natel EMS. "We appreciate the efforts of these suppliers and look forward to a mutually beneficial continued relationship in the future." The awards recognize the significant contributions of Natel suppliers as part of the company's product and performance achievement. The winners represent Natel's view, as the best the microelectronics/electronics industry has to offer in innovative technology, superior quality, outstanding launch support, crisis management and competitive total enterprise cost solutions. The suppliers of the Year winners are chosen by the Natel team of purchasing, engineering, quality, manufacturing and logistics executives.

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Tuesday, October 14, 2014

	INTERPOSERS & 3D PACKAGING	MODELING, DESIGN, & TEST	MATERIALS & PROCESSES	ADVANCED PACKAGING INTERCONNECTS & ASSEMBLY	FUTURE OF PACKAGING	SPECIAL SESSIONS: 3D & EMBEDDING, AND RELIABILITY
8:00 AM –11:10 AM	**TSV Materials & Processes** *Chairs: Vidhya Ramachandran, Qualcomm; Sesh Ramaswami, Applied Materials* Through Silicon Vias are key enablers for 3D integration with aggressive form factor and power/performance scaling. This session will focus on continuing efforts to address challenges in areas such as yield, reliability, manufacturability and cost effectiveness of advanced TSV integration.	**Design & Analysis for Reliability** *Chairs: Gopal Jha, Avago Technologies Inc.; John Pan, Cal Poly State University* Improvements in design and analysis methodologies are critical to understand and enhance product robustness during its life cycle under normal operating conditions. This session covers development in innovations in various design and analysis approaches for long term reliability improvement including the analysis of physics of failure, novel device/package/process/material designs, finite element modeling, and testability analysis.	**Advanced Materials & Novel Assembly Processes** *Chairs: Allan Beikmohamadi, DuPont; Yasuhiro Kawase, Mitsubishi Chemicals* A novel method for packaging using lid ties of encapsulation materials deposited in an array on the coreless flip chip laminate substrates will be introduced. Various progresses on multi-walled carbon nano particles, use of nano particles on reduction of sintering temperature, and package-on-package for automotive applications will be presented.	**Flip Chip - Solder** *Chairs: Mary Cristina Ruales Ortega, Universidad del Turabo; John Bolger, Department of Defense; Linlin Yang, Alta Devices* Flip Chip solder bumping is a reliable interconnect technology that is directly compatible with many of the latest semiconductor technologies, including 2D, 3D, organic packages, fanout, and ultra-thin packages. Continued reliability testing, process development, and new RoHS materials development are essential to ensure that solder bumping is a long-term interconnect solution as these new semiconductor technologies evolve.	**Future of Packaging** *Chairs: Erica Folk, Northrop Grumman; Nick Renaud-Bezot, AT&S AG* New, innovative packaging techniques are needed to support the growing need for smaller and more capable devices. This session covers industry needs, roadmaps and new technologies that are essential to drive the future of packaging.	**3D and Embedding** *Chairs: Doug Shelton, Canon USA, Inc.; Woong-Sun Lee, SK Hynix, Inc.* 3D and Embedded Device Technologies integrate passive and active components into versatile, efficient and compact 3D, 2.5D and Advanced Packaging designs that increase system functionality, reliability and IO density. This session addresses some of the challenges related to 3D and Embedded Device manufacturing including metrology, yield management, reliability and materials.

Tuesday, October 14, 2014

	INTERPOSERS & 3D PACKAGING	MODELING, DESIGN, & TEST	MATERIALS & PROCESSES	ADVANCED PACKAGING INTERCONNECTS & ASSEMBLY	FUTURE OF PACKAGING	SPECIAL SESSIONS: 3D & EMBEDDING, AND RELIABILITY
8:00 AM –8:25 AM	**Featured Speaker:** 3D IC Integration Using TSV-Last and Micro-Bumps Technologies *Nuno YC Chen, MTI (Macrotech Technology Inc.) (C.C Chang, Kiwi Chung, Tom Ni)*	**Featured Speaker:** Compressive-Post Packaging of Double-Sided Die *Woochan Kim, Virginia Tech (CPES) (Jia-Woei Wu, Sauvik Chowdhury, Nga Lee, Collin Hitchcock, James J.-Q. Lu, T. Paul Chow, Khai D.T. Ngo)*	**Featured Speaker:** Thermal and Reliability Demonstration of a Large Die, Low CTE Chip Scale Package *Sushumna Iruvanti, IBM (Masahiro Fukui, Kenji Terada, Tomoyuki Yamada, Charlie Reynolds, Rebecca Wagner, Yi Pan, Hilton Toy, Charles Carey, Kamal Sikka, Brian Sundlof)*	**Featured Speaker:** High Productivity Thermo-Compression Flip Chip Bonding *Bob Chylak, Kulicke and Soffa Industries, Inc. (Tom Colosimo, Matthew Wasserman, Michael Schmidt-Lange, Horst Clauberg, Patrick Desjardins)*	**Featured Speaker:** Packaging: Past, Current and Future *Rao Tummala, Georgia Tech 3D Systems Packaging Research Center (PRC)*	**Featured Speaker:** Fabrication of Through Substrate Vias Post Foundry to Support High reliability 2.5D Application *Joshua Luff, Honeywell FM&T (Jim Will)*
8:30 AM –8:55 AM	Impact of Through Silicon Via Scaling on Electrical and Mechanical structures in 20nm Test Vehicle *Sarasvathi Thangaraju, GLOBALFOUNDRIES (Sukesh Kannan, Daniel Smith; Vidhya Ramachandran, Dan Perry, Brian Henderson, Sam Gu, Riko Radojcic, Qualcomm)*	Methodology for Predicting BGA Warpage by Incorporating Metal Layer Design *Sandeep Shantaram, Freescale Semiconductor (Torsten Hauck)*	A Large Die Large Laminate Coreless Package using Lid Ties *Edmund Blackshear, IBM (Brian Quinlan, Benjamin Fasano, David Lewison, Shidong Li, Hugues Gagnon, Paul Fortier, Frederick Roy, Takeshi Nakajima, Yoichi Miyazawa, Itsuroh Shishido, Tomoyuki Yamada, Hilton Toy)*	Modeling of Fluid Phases During the Flip-Chip Placement and Joining Processes *Julien Sylvestre, University de Sherbrooke (David Benoit; Āric Duchesne, Maud Samson, IBM; Dominique Langlois-Demers, MiQro Innovation Collaboration Center)*	Electrical Characterization of Fibre-Reinforced Plastics by Atmospheric Plasma Technology *Rene Schramm, University Erlangen-Nuremberg, Institute for Factory Automation and Production Systems (FAPS) (Payam Daneschwar, Joerg Franke)*	Automated Metrology Improves Productivity and Yields for Wafer Level Packaging in High Volume Manufacturing *Russ Dudley, Rudolph Technologies (David Marx; Jin You Zao, Bong YY, Lim Beng Kuan, STATSChipPAC, Singapore)*
9:00 AM –9:25 AM	Impact of Grain Structure and Material Properties on Via Extrusion in 3-D Interconnects *Tengfei Jiang, University of Texas at Austin (Chenglin Wu, Jay Im, Rui Huang, Paul S. Ho)*	Parametric Studies of Effects of Solder Bump Pitch, Package Size, and Molding Compound and Substrate Thicknesses on Warpage of PBGA Packages *Sungbum Kang, Georgia Institute of Technology (I. Charles Ume)*	POP Technology for the Automotive Industry *S. Craig Beddingfield, Texas Instruments (Kurt Wachtler, David Chin)*	The Failure Behavior of the Fine Pitch SnAg Bump Under Current Stressing *Yu-Hsiu Shao, ASE (Advanced Semiconductor Engineering) (Ying-Ta Chiu, Chin-Lin Kao, Ping-Feng Yang)*	High Resolution Patterning Technology to enable Panel Based Advanced Packaging *Klaus Ruhmer, Rudolph Technologies, Inc. (Philippe Cochet, Rajiv Roy, Elvino De Silveira, Rich Rogoff)*	Reliability of Multi-Layer Wiring Board Embedded with Two Dies in Stacked Configuration *Koji Munakata, Fujikura Ltd. (Nobuki Ueta, Masahiro Okamoto, Kumi Onodera, Kazuhisa Itoi, Satoshi Okude and Osamu Nakao; Theodore Tessier, Flip Chip International, LLC)*
9:30 AM – 9:55 AM	Impact of Bath Stability on Electroplated Cu for Through-Silicon-Vias (TSV) in a Controlled Manufacturing Environment *Anh Nguyen, College of Nanoscale Science and Engineering, SUNY (Kevin Fealey, Peter Reilly, Gyanaranjan Pattanaik, Alison Gracias, Fred Wafula, Michael Flynn, Jack Enloe)*	Vibration Testing as a Tool to Optimize the Configuration of the PCBs *Ivan Szendiuch, Brno University of Technology (Psota B., Otahal A., Klapka M.)*	Correlation Between Thermo-mechanical Reliability and Superhydrophobic Nature of CNT Composite Coatings *Yoonchul Sohn, Samsung Advanced Institute of Technology (Dongouk Kim, Sangeui Lee, Jae Yong Song, Sunghoon Park, Hajin Kim, Youngchul Ko, Kunmo Chu, Intaek Han)*	Fine Pitch Copper Pillar Interconnection with C4 (Mass Reflow) Processing *Fernando Roa, Amkor Technology*	SNaP: A Process for Achieving Adhesion between Electroless Copper and Dielectrics with Minimal Surface Roughening *Meng Hsieh, Atotech USA (Ellina Libman, Lutz Brandt)*	Solderable Anisotropic Conductive Adhesives for 3D Package Application *Wusheng Yin, YINCAE Advanced Materials, LLC (Mary Liu)*

COFFEE BREAK IN FOYER: 9:55 AM – 10:15 AM **IMAPS Cafés sponsored by:** Invensas™

Tuesday, October 14, 2014

	INTERPOSERS & 3D PACKAGING	MODELING, DESIGN, & TEST	MATERIALS & PROCESSES	ADVANCED PACKAGING INTERCONNECTS & ASSEMBLY	FUTURE OF PACKAGING	SPECIAL SESSIONS: 3D & EMBEDDING, AND RELIABILITY
10:15 AM –10:40 AM	Backside Exposure of Small-sized TSVs using Si/Cu Grinding, CMP, Cap Layer Deposition, and Alkaline Etching *Naoya Watanabe, National Institute of Advanced Industrial Science and Technology (Masahiro Aoyagi, Daisuke Katagawa, Tsubasa Bandoh, Eiichi Yamamoto)*	Analysis of Crack Length and Crack Position in the Solder Joints of High Power LEDs by Transient Thermal Measurements and Finite Element Simulations *Shri Vishnu Kandaswamy, Technische Hochschule Ingolstadt*	Pressureless Sintering of Nano-Ag Paste with Low Porosity for Die Attach *Ning-Cheng Lee, Indium Corporation (Sihai Chen, Guangyu Fan, Xue Yan, Lee Kresge, Chris LaBarbera)*	Impact of Reprocessing Technique on First Level Interconnects of Pb-Free to SnPb Reballed Area Array Flip Chip Devices *Joelle Arnold, DfR Solutions (Melissa Keener, Steph Gulbrandsen, Nathan Blattau, David Kayser, Greg Caswell)*	Z-Interconnect Technology - A Reliable, Cost Efficient Solution for High Density, High Performance Electronic Packaging *John Lauffer, i3 electronics (Kevin Knadle)*	Highly Sophisticated Microsystems with Heterogeneous Embedding Technologies *Christian Boehme, Fraunhofer IZM (Stephan Benecke, Andreas Ostmann)*
10:45 AM –11:10 AM	Cost Analysis of TSV Process and Scaling Options *Larry Smith (Klaus Hummler, Steve Olson, Brian Sapp, Victor Vartanian, Tyler Barbera, Steve Golovato, Kai-Hung Yu, Toshio Hasegawa, Shan Hu, Gert Leusink, Kaoru Maekawa, Jack Enloe, Alison Gracias, Gyanaranjan Pattanaik, Fred Wafula)*	Solder Joint Reliability Assessment for a High Performance RF Ceramic Package *Paul Charbonneau, Sanmina Corporation (Hans Ohman, Marc Fortin)*	High Temperature Viable Interconnection Realized by Sintering Nano Solder at Low Temperature *Ying Zhong, Harbin Institute of Technology & UCSD (Chunqing Wang, Sungho Jin)*	Consumable Anode Process for SnAg Electroplating *Marvin Bernt, Applied Materials (Adam McClure)*	Wafer Dicing Using Dry Etching on Standard Tapes and Frames *David Lishan, Plasma-Therm LLC (Thierry Lazerand, Ken Mackenzie, David Pays-Volard, Linnell Martinez; Gordy Grivna, Jason Doub, ON Semiconductor)*	Adhesive Enhancement Technology for Directly Metal Plating on EMC *Kenichiroh Mukai, Atotech USA Inc. (Kwonil Kim, Brian Eastep, Lee Gaherty, Anirudh Kashyap)*

San Diego Skyline

Tuesday, October 14, 2014

Opening Ceremonies: Annual Business Meeting, Awards Ceremony, Keynote

11:00 AM - 5:00 PM: Exhibit Hall Opens
11:25 AM - 11:40 AM: Annual Business Meeting
11:40 AM - 12:00 PM: IMAPS Society Awards Ceremony

Daniel C. Hughes, Jr. Award
William D. Ashman Award
John A. Wagnon, Jr., Technical Achievement Award
IMAPS Fellow of the Society
Outstanding Educator Award
Sidney J. Stein International Award
Corporate Recognition Award
President's Awards
Outstanding Papers - IMAPS 2013
Best Paper - IMAPS 2013
Steve Adamson Memorial Award

Come say Thank You to those who contributed so much to IMAPS over many years.

KEYNOTE:

12:00 PM - 12:45 PM

Classical Packaging - Its Strengths, Limitations, and Innovation Drivers

The semiconductor packaging roadmaps have been veering towards an inflexion point over the last few years. Competing and somewhat orthogonal demands of the mobile revolution, internet of things (IoT) and the potential "slowdown" of Moore's law has been driving many new trends and innovations in packaging. The applications space, i.e., end use constraints require "out of box" thinking even in "classical packaging" such as wire bonding or large body LGA packages. I will discuss key trends based on business applications and summarize advantages and challenges with a "call to arms" for innovation.

Dr. Steve Bezuk *is Senior Director of IC Package Engineering at Qualcomm. Steve's group is responsible for current and future generations of packaging technologies for all of Qualcomm's wireless applications. Prior to joining Qualcomm Steve was with Kyocera, Unisys, Sperry-Univac and RCA's Sarnoff Research Center. Steve has worked and managed groups in a variety of areas, including of amorphous silicon research, CMOS, Bipolar and GaAs IC process development, Laser enhanced materials processing, and wirebond, TAB, Flip Chip, MEMS, and TSV packaging.*

Steve is also very active in the IEEE CPMT and is their current VP of Technology. Steve is also active with the ECTC Conference for the society and was the General Chair for the 2004 ECTC conference and is the Current Publications Chair.

Steve has a B.S. in Chemistry from the University of Pittsburgh and a Ph.D. in Chemistry from the University of Minnesota.

12:45 PM - 2:00 PM: Lunch Break

Tuesday, October 14, 2014

	INTERPOSERS & 3D PACKAGING	MODELING, DESIGN, & TEST	MATERIALS & PROCESSES	ADVANCED PACKAGING INTERCONNECTS & ASSEMBLY	FUTURE OF PACKAGING	SPECIAL SESSIONS: 3D & EMBEDDING, AND RELIABILITY
2:00 PM –6:25 PM	**Interposers/3D Integration - I** *Chairs: Urmi Ray, Qualcomm; Kyu-oh Lee, Intel Corporation* This session will present highlights of integration challenges and solutions for interposers/3D packaging arena.	**Modeling & Design for SI, PI and EMC** *Chairs: Ege Engin, San Diego State University; Gabriel Parès, CEA LETI* Electrical design of interconnects and packaging are essential for high-speed digital and high-frequency analog systems. This session covers modeling, simulation, and design techniques to ensure SI/PI/EMC.	**Polymers, Underfill, Encapsulants & Adhesives** *Chairs: Jeff Gotro, InnoCentrix; Lyndon Larson, Dow Corning* This session introduces innovative polymeric solutions to a variety of uses such as underfill, thick film, molding, and die attach adhesive applications.	**Wirebonding & Stud Bumping** *Chairs: Dan Evans, Palomar Technologies; Lee Levine, Process Solutions Consulting* Wire bonding continues as a dominant method of chip interconnection. This session covers novel surface analysis and preparation processes and advancements in Copper and Silver wire bonding for both ball and wedge bonding of fine and heavy wire. Packaging engineers will find this session helpful to explore alternative design choices for selecting wire bond materials, processes, and test methods.	**Medical Device Packaging** *Chairs: Andre Rouzaud, CEA/Léti; Susie Johansson, Starkey Hearing* Medical devices are some of the most complex and cutting-edge products available today. This session will address new packaging developments taking into account the very specific and severe constraints linked to different medical applications (in vivo, in vitro, pharmaceutical…).	**Reliability I** *Chairs: Aicha Elshabini, University of Idaho; Stevan Hunter, ON Semiconductor* The reliability session covers fabrication of through substrate vias post foundry to support High reliability 2.5D application, automated metrology improving productivity and yields for wafer level packaging in high volume manufacturing, reliability of multilayer wiring board embedded with two dices in stacked configuration, solderable anisotropic conductive adhesives for 3D package application, highly sophisticated microsystems with heterogeneous embedding technologies, challenges and solutions in preparation for high resolution failure analysis of power electronics, heavy-wire bond manipulation with laser to increase reliability and as enabler for thermography based online process control, reliability of PCB solder joints assembled with SACM0510 solder paste, and quality monitors and inspection criteria for bare die and bare die PoP packages.
2:00 PM –2:25 PM	**Featured Speaker:** Comparison of Measured and Modeled Lithographic Process Capabilities for 2.5D and 3D Applications Using a Step and Repeat Camera *James Webb, Rudolph Technologies, Inc. (Steven Gardner, Roger McCleary; Gerald Lopez, Gen1Sys, Inc.)*	**Featured Speaker:** Ceramic Process Variation Impact on Electrical Design of High Frequency and High Speed Interconnects and Components *Jerry Aguirre, Kyocera America, Inc (Paul Garland, Hiroshi Makino)*	**Featured Speaker:** Thermally Conductive Capillary Underfill for Advanced Flip Chip Bonding Applications *Naichao Li, 3M (Guoping Mao, Eric Larson, Blake Dronen)*	**Featured Speaker:** Effect of Process Parameters on Free Air Ball Integrity in Copper and Palladium-coated Copper Bonding Wire *Noritoshi Araki, Nippon Micrometal Corporation (Yasutomo Ichiyama, Ryo Oishi, Teruo Haibara, Takashi Yamada)*	**Featured Speaker:** SiP with TSV for Class 1 Medical Devices *Doug Link, Starkey Hearing Technologies*	**Featured Speaker:** Challenges and Solutions in Preparation for High Resolution Failure Analysis of Power Electronics *R. Klengel, Fraunhofer Institute for Mechanics of Materials IWM (B. Boettge, S. Klengel)*
2:30 PM –2:55 PM	A Solution to Remove Temporary Bonding Materials in Through-holes in Bottom-up Electroplating Process *Zijian Wu, Tsinghua University*	New Method for Mitigating Weave-induced Differential Skew in PWBs *Taiga Fukumori, Fujitsu Laboratories Ltd. (Tomoyuki Akahoshi, Daisuke Mizutani, Motoaki Tani)*	Pre-applied Inter Chip Fill for 3D-IC Joining *Yasuhiro Kawase, Mitsubishi Chemical Corporation (Masaya Sugiyama, Makoto Ikemoto, Hideki Kiritani, Fumikazu Mizutani, Keiji Matsumoto, Hiroyuki Mori, Yasumitsu Orii)*	Advancement in Thermosonic Bonding Wire *Sarangapani Murali, Heraeus Materials Singapore Pte Ltd. (Zhang Xi)*	Mechanical Reliability of Ceramic Packages for Active Implantable Medical Devices - The IEC Hammer Test *Fabian Kohler, Laboratory for Biomedical Microtechnology, BrainLinks-BrainTools Cluster of Excellence (ExC1086), University of Freiburg (Thomas Stieglitz, Martin Schuettler)*	Packaging Design and Assembly for Ultrahigh Energy Density Microbatteries *Caroline Bjune, Charles Stark Draper Laboratory (Thomas Marinis, Yet-Ming Chiang)*

Tuesday, October 14, 2014

	INTERPOSERS & 3D PACKAGING	MODELING, DESIGN, & TEST	MATERIALS & PROCESSES	ADVANCED PACKAGING INTERCONNECTS & ASSEMBLY	FUTURE OF PACKAGING	SPECIAL SESSIONS: 3D & EMBEDDING, AND RELIABILITY
3:00 PM –3:25 PM	Multi-scale X-ray Tomography for Process and Quality Control in 3D TSV Packaging *Ehrenfried Zschech, Fraunhofer IKTS (Sven Niese, Markus Loeffler, Juergen Wolf)*	PWB Z Interconnect Technology - Electrical Performance *Chase Carver, i3 Electronics (Norman Seastran, Robert Welte)*	Epoxy Underfill Challenges for Narrow Pitch Copper (Cu) Pillar Solder Bump Packages *Brian Schmaltz, NAMICS Technologies*	Fine Pitch Cu Wire Bonding Capability - Process Optimization and Reliability Study *Ivy Qin, Kulicke and Soffa Industries, Inc. (Hui Xu, Cuong Huynh, Bob Chylak; Hidenori Abe, Dongchul Kang, Yoshinori Endo, Masahiko Osaka, Shinya Nakamura, Hitachi Chemical)*	Thick Film Technology For Today's Hearing Products *John Dzarnoski, Starkey Hearing Technologies (Susie Johansson)*	Comparison of Different Methods for Stress and Deflection Analysis in Embedded Die Packages During the Assembly Process *Katerina Macurova, Materials Center Leoben Forschung GmbH (Raul Bermejo, Martin Pletz, Ronald Schöngrundner, Thomas Antretter, Thomas Krivec, Mike Morianz, Michel Brizoux, Wilson Maia)*
	DESSERT "HAPPY HOUR" & COFFEE BREAK IN EXHIBIT HALL (GRAND BALLROOM): 3:25 PM - 4:30 PM **IMAPS Cafés sponsored by:** Invensas™ **Dessert "Happy Hour" Sponsor:** PALOMAR™ TECHNOLOGIES					
4:30 PM –4:55 PM	Buried Secrets - Embedding as Support for More-than-Moore *Nick Renaud-Bezot, AT&S AG*	Thermal and EMI Performance Evaluation of Composite Plastic Molded Heat Sinks and Hybrid TIM Materials *Alpesh Bhobe, Cisco Systems (Herman Chu, Xiao Li, Lynn Comiskey)*	Performance Assessment of a Low Temperature Polymer Conductor for Lead-Free Soldering Processes *Steven Grabey, Heraeus Precious Metals (Samson Shahbazi, Sarah Groman, Catherine Munoz)*	Experimental and Numerical Simulation Study of Pre-Deformed Heavy Copper Wire Wedge Bonds *Andreas Unger, University of Paderborn (Walter Sextro, Simon Althoff, Paul Eichwald, Tobias Meyer, Michael Brokelmann, Daniel Bolowski)*	Embedded Capacitive Filter Units in LTCC for the Protection of Active Implantable Devices *Juan Ordonez, Laboratory for Biomedical Microtechnology, BrainLinks-BrainTools Cluster of Excellence (ExC1086) (Vivek Singh, Fabian Kohler, Jenny Pfau, Martin Schuettler, Thomas Stieglitz)*	Development of Simulation Tool to Predict Deflection of Small-Sized Chip by Wire Bonding USG *Jongwan Kim, Samsung Electronics (Hyuksu Kim, Kwangyul Lee, Taeduk Nam, Junyoung Oh)*
5:00 PM –5:25 PM	Efficient Non-reagent Metrology for Modern TSV Baths *Michael Pavlov, ECI Technology (Gene Shalyt, Danni Lin)*	Hashing Processors: A New Challenge for Power Package Design *Thomas Tarter, Package Science Services LLC (Wayne Nunn, Andy Carrasco, PSS; Humair Mandavia, Brad Garafolo, James Church, Zuken)*	Reliability Potential of Silicone Molding Compound for LED Application *Yue Shao, University of California, Irvine*	Gold Wirebond on Discolored Bond Pads *Stevan Hunter, ON Semiconductor, and Idaho State University (Hasaan Masood, Durgasamanth Pidikiti, Qutaiba Khalid, D. Subbaram Naidu)*	Advanced Electronic Packaging Options for Miniaturization of Complex Medical Devices *Susan Bagen, Micro Systems Technologies, Inc.*	Enhanced Thermal Management Solutions for RF Power Amplifiers *Brooke Locklin, Element Six Technologies (Felix Ejeckam, Daniel Twitchen, Thomas Obeloer, Bruce Bolliger)*
5:30 PM –5:55 PM	A New Package Structure for High Speed eStorages *Hyejin Kim, Samsung Electronics (Sunghoon Chun, Jaeyeon Hwang, Ilmok Kang)*	Causality Enforcement Via Periodic Continuations for High-speed Interconnects *Lyudmyla Barannyk, University of Idaho (Hazem Aboutaleb, Aicha Elshabini, Fred Barlow)*	One Step Chip Attach Materials (OSCA) for Conventional Mass Reflow Processing *Daniel Duffy, Kester Inc.*	Reliability Assessment of Flip-Chip Assembly of Al Bumps *Hidekazu Tanisawa, R&D Partnership for Future Power Electronics Technology (Kohei Hiyama, Takeshi Anzai, Hiroki Takahashi, Yoshinori Murakami, Shinji Sato, Hiroshi Sato, Fumiki Kato, Kinuyo Watanabe)*	Metallization and Chip Bonding Processes for Wearable Electronics Packaging with Stretchability *Tae Sung Oh, Hongik University (J.Y. Choi, D.W. Park, W.J. Kim)*	Heavy-Wire Bond Manipulation with Laser to Increase Reliability and as Enabler for Thermography based Online Process Control *Andreas Middendorf, Fraunhofer IZM (Astrid Gollhardt, Amrita Bohn, Klaus Dieter Lang)*
6:00 PM –6:25 PM	Package-on Package-Design for Size Reduction and Assembly Process Development *Syed Sajid Ahmad, Center for Nanoscale Science and Engineering, NDSU (Mike Reich, Fred Haring, Aaron Reinholz)*	Correlation of Warpages and Reliability Characteristics of Package-on-Packages *Tae Sung Oh, Hongik University (D.H. Park, D.M. Jung, J.Y. Choi; L. Fabiano, C. Moraes, Unisinos Univ., Brazil)*	Size Effect of Particulate Filler on Electrical Resistivity of Carbon Nanotube Polymer Composites: Transition of Excluded Volume Effects *Sunghoon Park, Samsung Advanced Institute of Technology (SAIT)*	CO2 Spray Cleaning and OSEE Non-Contact Surface Inspection for Wire Bond Pad Preparation *David Jackson, CleanLogix LLC*		Reliability of PCB Solder Joints Assembled with SACM0510 Solder Paste *Ning-Cheng Lee, Indium Corporation (Arnab Dasgupta, Fengying Zhou, Weiping Liu, Paul Bachorik, Christine LaBarbera)*

Wednesday, October 15, 2014

	INTERPOSERS & 3D PACKAGING	MODELING, DESIGN, & TEST	MATERIALS & PROCESSES	ADVANCED PACKAGING INTERCONNECTS & ASSEMBLY	FUTURE OF PACKAGING	SPECIAL SESSIONS: 3D & EMBEDDING, AND RELIABILITY
8:00 AM –11:25 AM	**Glass Interposers** *Chairs: Steve Annas, Triton MicroTech; Aric Shorey, Corning* The use of glass as a semiconductor substrate continues to mature. In this session, significant progress in development of the manufacture of glass interposers in wafer and panel format will be presented.	**Thermal and Thermo-Mechanical Modeling** *Chairs: Kamal Sikka, IBM Systems & Tech Group; Bill Marsh, Northrop Grumman ES* This session deals with experiments and simulations related to thermal management of GaN transistors, 3D die stacks, automotive inverters and avionic file servers.	**Substrate Materials and Technology** *Chairs: Michael Folk, Northrop Grumman; Anwar Mohammad, Flextronics; Kiran Vanam, Qualcomm* Substrate materials and associated processes must evolve to support both current needs and the future needs of packaging. In this session, emerging substrate materials and related manufacturing technologies will be presented.	**Electronic Packaging for Harsh Environment and Hi-Reliability (Mil/Aero)** *Chairs: Benson Chan, i3 Electronics, Inc.; Sergei Zotov, University of CA, Irvine* Covers a wide scope and include detailed experimental analysis of electronic packages and elements of the packages operating under harsh environments, including a wide range of temperatures and vibration levels.	**MEMS and Sensors Packaging** *Chairs: Matt Apanius, SMART Microsystems; Julie Adams, UBOTIC Company; Igor Prikhodko, Analog Devices* Challenges of MEMS and Sensor packaging related to specific applications will be discussed. This session includes environmental sensors, hermetic packaging, microfluidics, and advanced interconnect schemes.	**Reliability II** *Chairs: Martin Schneider-Ramelow, Fraunhofer IZM; Susan Bagen, Micro Systems Technologies, Inc.* This session covers a wide scope of reliability topics touching on the subjects of verification of parts, design reliability and harsh environments.
8:00 AM –8:25 AM	**Featured Speaker:** Comparison of Fabrication Process Capability and Electrical Performance with Silicon and Glass Interposers *Satoru Kuramochi, Dai Nippon Printing (Sumio Koiwa, Takamasa Takano, Kosuke Suzuki, Yoshitaka Fukuoka)*	**Featured Speaker:** Advanced Thermal Dissipation in GaN-on-Diamond Transistors *Rusen Yan, University of Notre Dame (Yuanzheng Yue, Grace Xing, University of Notre Dame; Felix Ejeckam, Bruce Bolliger, Element Six Technologies)*	**Featured Speaker:** Precision Solder Paste Jetting of Solder Paste - a Versatile Tool for Small Volume Production *Karl-Friedrich Becker, Fraunhofer IZM (M. Koch, S. Voges, J. Bauer, T. Braun, R. Aschenbrenner, M. Schneider-Ramelow, K.-D. Lang)*	**Featured Speaker:** Effects on the Reliability of Lead-Free Solder Joints Under Harsh Environment *Zhou Hai, Auburn University (Jiawei Zhang, Chaobo Shen, John Evans, Micheal Bozack)*	**Featured Speaker:** 160 Milliohm Thru-Wafer Interconnects with 10:1 Aspect Ratio *Alexandra Efimovskaya, University of California, Irvine (Andrei Shkel)*	**Featured Speaker:** Quality Monitors and Inspection Criteria for Bare Die and Bare Die PoP Packages *Kiran Kumar Vanam, Qualcomm (Anthony Newman)*
8:30 AM –8:55 AM	Development of Glass Interposer with Fine Pitch Micro Bumps and Bow Study Depending on Several Glass Substrates with Differential CTE *Kenichi Mori, Shinko Electric Industries Co., Ltd.*	Suppressing the Hot Spot Temperature in 3-D ICs Using All-Carbon Thermal Management Approach *Linjuan Huang, University of California, Irvine*	Advanced Build-up Materials and Processes for Packages with Fine Line and Space *Hirohisa Narahashi, Ajinomoto Fine Techno*	High Temperature Reliability of Copper Wire-Bonded Packages Encapsulated with Mold Compounds Containing Sulfur Compounds *Varughese Mathew, Freescale Semiconductor Inc. (Sheila Chopin)*	Packaging MEMS and Printed Gas Sensors: Merging Two Worlds *Joe Stetter, KWJ Engineering Inc. (Edward Stetter, Spec Sensors LLC)*	SigNature DNA Marking: The Authentication Platform DLA has Selected as Part of their Counterfeit Prevention Effort for Electronics *Janice Meraglia, Applied DNA Sciences*
9:00 AM –9:25 AM	Glass Substrates for Advanced Packaging *Aric Shorey, Corning Inc. (Scott Pollard)*	Thermal Modeling of Large Embedded GaN Transistors *John Roberts, GaN Systems Inc. (J. Roberts, G. Klowak, Nick Renaud-Bezot, L. Yushyna)*	The Impact of Hydrogen Gas Evolution on Blister Formation in Electrolessly Deposited Copper Films *Tobias Bernhard, Atotech Deutschland GmbH (Lutz Stamp, Frank Bruening; Ralf Bruening, Tanu Sharma, Mount Allison University)*	Packaging Induced Die Stress Characterization Between -180ºC and 80ºC Using van der Pauw Sensors *Uday S. Goteti, Auburn University (Francy Akkara, Richard Jaeger, Michael Hamilton, Jeffrey Suhling)*	A Resealable Hermetic Packaging Technique for Silicon Microfluidic Devices *Lilla Safford Smith, UC Berkeley (Gordon Hoople, Jim Cheng; Albert Pisano, UC San Diego)*	Composition and Form: How Feedthrough Design Affects Package Reliability *Richard Share, Share Consulting, LLC*

COFFEE BREAK IN EXHIBIT HALL (GRAND BALLROOM): 9:25 AM - 10:00 AM
(Exhibit Hall Open (GRAND BALLROOM): 9:00 AM - 7:30 PM)

IMAPS Cafés sponsored by:

Wednesday, October 15, 2014

	INTERPOSERS & 3D PACKAGING	MODELING, DESIGN, & TEST	MATERIALS & PROCESSES	ADVANCED PACKAGING INTERCONNECTS & ASSEMBLY	FUTURE OF PACKAGING	SPECIAL SESSIONS: 3D & EMBEDDING, AND RELIABILITY
10:00 AM –10:25 AM	Adhesion Enabling Technology for Reliable Metallization and Patterning of Glass Interposers *Sara Hunegnaw, Atotech USA Inc. (Lutz Brandt, Hailuo Fu, Zhiming Liu, Tafadzwa Magaya)*	Thermal Management Solutions for Network File Server Used in Avionics Applications *Vicentiu Grosu, Teledyne Controls (Chris Lindgren, Tamas Vejsz, Teledyne Controls; Ya-Chi Chen, Avijit Bhunia, Teledyne Scientific)*	Recent Technologies of Solder Resist Process of FCCSP for Advanced Interfacial Properties Between Chip and Substrate *Changbo Lee, Samsung Electro-Mechanics (Myeong-ho Hong, Jeongho Yeo)*	Analyses of PBGA Packaging Reliability under Strong Vibration *Yeong Kim, Inha University (Dosoon Hwang)*	Design of a Miniaturized Vibrating Beam Power Converter *Thomas Marinis, Draper Laboratory (Joseph Soucy)*	New Fabrication Process for the Manufacture of Hi Reliability Space Electronics *Carl Edwards, Space Micro Inc.*
10:30 AM –10:55 AM	Low Cost Glass Interposer Development *Yu-Hua Chen, Unimicron Technology Corp. (Shaun Hsu, Dyi-Chung Hu; Urmi Ray, Ravi Shenoy, Kwan-Yu Lai, Qualcomm Technologies, Inc.; Aric Shorey, Rachel Lu, Windsor Thomas III, Corning Inc.)*	Air-Cooled Heat Exchanger for High-Temperature Power Electronics *Scot Waye, National Renewable Energy Laboratory (Jason Lustbader, Matthew Musselman, Charles King)*	New Liquid Crystal Polymer Substrate for High Frequency Applications *Michael Zimmerman, iQLP (Meredith Dunbar, Deepukumar Nair, Keith Smith, Rich Wessel)*	Importance of Effective Root Cause Analysis of Failures in High Reliability Microelectronics Applications - Case Studies *Gwen Schulz, Honeywell*	Dynamic Moisture Model In A Hermetic Package With Active Moisture Absorbing/Desorbing Materials *Benjamin Decker, Northrop Grumman (Randall Lewis, Steve Smalley, Kevin McGrath, Eric Schoch, Len Chorosinski)*	Large Form Factor Hybrid LGA Interconnects; Recent Applications and Technical Learning *John Torok, IBM Corporation (Brian Beaman, William Brodsky, Shawn Canfield, Jason Eagle, Mark Hoffmeyer, Theron Lewis, Yuet-Ying Yu)*
11:00 AM –11:25 AM	High Reliability and High Performance 30um Through-Package-Vias in Ultra-Thin Bare Glass Interposer *Venky Sundaram, Georgia Tech PRC (Jialing Tong, Kaya Demir, Timothy Huang, Rao Tummala; Aric Shorey, Scott Pollard, Corning, Inc.)*		Fast Etching of Microscale Structures by Bombardment with Electrosprayed Nanodroplets *Enric Grustan-Gutierrez, University of California, Irvine (Rafael Borrajo-Pelaez, Manuel Gamero-Castaño)*	Characterization of Thermally Induced Stress in IC packages Over a Temperature Range of -180ºC to 80ºC Using PiFET Stress Sensors *Francy Akkara, Auburn University (Uday Goteti, Richard Jaeger, Michael Hamilton, Jeffrey Suhling)*	Development of a Semiconductor Gas Sensor Integrated in LTCC for Detection of Explosive and Toxic Gases *Hansu Birol, CSEM Brasil (G. Farine, T. Maeder, P. Ryser, V. Zanchin, S. Lopera, S. Orlando, L.O.S. Cesar, E. Gyoervary, D. Wolin, T. Alves)*	High Temperature Resistant Interconnection by Using Nano Nickel Particles *Yasunori Tanaka, Waseda University / Tatsumi Lab. (Suguru Hashimoto, Tomonori Iizuka, Kohei Tatsumi, Norie Matsubara, Shinji Ishikawa, Masamoto Tanaka)*

Wednesday, October 15, 2014
KEYNOTE:

11:30 AM – 12:15 PM

High-end Packaging Development: Opportunities and not Challenges

As silicon scaling has reached an asymptote, Packaging is now the key driver for increasing System bandwidth and performance. With Big Data and Analytics driving business decisions, high-end mainframes form the backbone of complex Cloud-based data-centers. After tracing the history of high-end Packaging, this keynote address will describe the opportunities available at the package and System level to drive the next-generation compute models. Opportunities span new packaging form-factors, advanced materials and complex assembly processes. Underlying such development is a need for unified testing and modeling standards.

Dr. Kamal Sikka *is the manager of the Systems Scaling unit process and materials development team at IBM Microelectronics, with responsibilities related to technology development for high-end 2D and 3D packaging. He obtained his PhD degree in Mechanical Engineering from Cornell University in 1997. Dr. Sikka has received several formal IBM awards, published over 30 technical papers and holds 27 patents.*

12:15 PM - 1:30 PM: Lunch in Exhibit Hall (GRAND BALLROOM)
(Lunch Kiosks – Food not Provided by IMAPS)

GLOBAL BUSINESS COUNCIL (GBC) Luncheon & Marketing Forum

Wednesday, October 15, 2014 | 12:15pm – 2:00pm

iMAPS Global Business Council

"The Future of Packaging: Mobile & Solar PV Markets"

12:15 PM: Lunch Begins

12:30 PM: Welcome, GBC Objectives and Agenda Review - Lee Smith, Plexus Corp.

12:40 - 1:10 PM:

The Future of Mobile Packaging and Integration Challenges

An exponential growth in the mobile phone, tablets and computing industry during the last decade has rapidly driven innovations in advanced packaging and integration. Smart integration at reasonable cost is a key to driving advanced functionality to mass market quickly. This has driven many new trends including architectural innovation for low power, technological innovations such as 2.5D, 3D as well as cost/price/manufacturing productivity innovations. Technology development challenges include tools, materials, infrastructure, reliability and many more. Several key challenges must be overcome before these integrations can be realized in a cost-effective manner. Current R&D and industry status will be presented, including technical, cost, business, standards and other factors important for rapid technology adoption.

Nick Yu, Vice President of Engineering, Qualcomm's CDMA Technologies Division

Nick is currently responsible for setting Qualcomm's semiconductor technology roadmaps including wafer fab process node, backend interconnect and packaging technologies. He manages engineering teams that are involved with our supply chain partners on execution of the technology roadmaps for Qualcomm's chipset products. Nick has 18 years of experience with Qualcomm on low power wireless chipset and SoC development, including managing chipset design, advanced semiconductor technology, deep submicron circuit design and methodology development, advanced semiconductor R&D and packaging development. He is one of the architects of, and has participated in the definition and development of, many Qualcomm chipset products. Nick has an MSEE degree from Georgia Institute of Technology.

1:10 PM - 1:40 PM:

Future Solar PV Module Fabrication Challenges and Opportunities in Brazil

Brazil, a country that recently went from the 9th to the 6th largest economy in the world, with an impressive growth rate that weathered the global crisis, and with a projected need for at least another 10GW of electricity generation capacity in the next decade, currently only has on the order of 10MW of installed grid-connected solar. While there are several reasons for this, the landscape for acceptance of solar PV has recently begun to change. For a country that has been electrical energy independent based on renewables for decades, this is a natural evolutionary step.

From the installation of solar panels on World Cup stadiums, to solar specific energy auctions, to plans to make the 2016 Olympics in Rio the greenest in history, Brazil is heading to the forefront of the charge to implement solar energy on a scale that makes an impact on national energy generation. And this is occurring in one of the largest untapped solar markets in the world.

This talk will deal with the changes in the financial, regulatory and environmental conditions affecting the acceptance and growth of solar PV in Brazil's energy matrix, focusing on the challenges and opportunities throughout the value chain in the industry and the market.

David Wolin, Director of Technology and Production, CSEM Brasil

David has been working on photovoltaic devices and systems for over 30 years in both major corporations and small enterprises. For the last seven years, he has been involved in bringing new solar photovoltaic technologies to Brazil, and in improving the business climate for their fabrication and installation in the country. Currently he is responsible for establishing the world's largest OPV pilot production capability in Belo Horizonte, Minas Gerias, Brazil.

1:40 – 2:00: Question & Answer Session and Closing Remarks

Moderated by Lee Smith, Chair

Wednesday, October 15 | 12:30pm - 2:00pm in the Exhibit Hall
Interactive Poster Session

Chair: Ben Decker, Northrop Grumman

One-on-One Interactive Forum. This is your chance for detailed interaction with industry and university authors whose work is too good to miss.

Synthèse, Caractérisation Et Mise En Œuvre D'un Matériau Hybride Organique-Inorganique Photosensible De Type Résine Positive. Application À La Fabrication Des Dispositifs Microfuidiques Par Écriture Laser
Elias Mechref, Laboratoire Charles Coulomb

Solution-Processed Metal Oxide Nanowire Mesh Electrodes for Efficient Solar Hydrogen Production from Water
Alireza Kargar, University of California, San Diego

Solar Tracking System
Nhat Vu, Temple University (Huan Le, Joan Delalic, Son Nguyen)

Power QFN Down Bond Area Delamination Mechanism Study
ZhiJie Wang, Freescale Semiconductor (China) Ltd. (Xu YanBo, ZongFei, J.Y. Niu, Hans Zhang)

Automatic Segmentation Method for Segmenting Chip Package and PWB Regions during Warpage Measurement of Unpainted PWB Assembly
Sungbum Kang, Georgia Institute of Technology (I. Charles Ume)

Custom Thickness Bare Die Availability of Any Product Through Device Extraction, Thinning, and UBM Pad Re-Conditioning
Erick Spory, Global Circuit Innovations, Inc.

Managing Voids in Adhesives for Medical Devices
Mary Ruales, Universidad del Turabo

Wednesday, October 15, 2014

	INTERPOSERS & 3D PACKAGING	MODELING, DESIGN, & TEST	MATERIALS & PROCESSES	ADVANCED PACKAGING INTERCONNECTS & ASSEMBLY	FUTURE OF PACKAGING
2:00 PM –5:55 PM	**Interposers/ 3D Integration - II** *Chairs: John Hunt, ASE US Inc.; Tolga Tekin, Fraunhofer IZM* Manufacturing technologies and methods used in the fabrication of 2.5D interposer and 3D silicon packaging	**Testing Methods and Process** *Chairs: Akhlaq Rahman, Thin Film Technology Corporation; Jim Will, Honeywell* Novel non-destructive characterization and product test screening techniques.	**LTCC and Ceramic Substrate Technologies** *Chairs: Daniel Krueger, Honeywell; Ken Peterson, Sandia National Labs.* This session explores the continuing innovation of processing, design, and application of ceramic and low temperature cofired ceramic (LTCC) packaging. Characterization of processes, new materials, design approaches, and novel device structures are explored. New advances in LTCC will be shared and of interest to designers, process engineers, and those interested in learning more about the application space of this technology.	**Novel Wafer Finish Processes** *Chairs: Ron Jensen, Honeywell; Rajiv Roy, Rudolph Technologies* Processes and technologies associated with wafer finish such as bumping and post-saw including novel technologies and approaches to thin-wafer handling.	**Power Packaging** *Chairs: Mark Hoffmeyer, IBM; Doug Hopkins, North Carolina State University; Fred Barlow, University of Idaho* This session presents zero stress die-attach for wide band gap semiconductor power devices, and interconnect and packaging techniques for system integration of high power assemblies. Additional topics will be covered such as capacitors, plast packages, SiC, multichip power module, and packaging development and construction for efficient extreme current power delivery.
2:00 PM –2:25 PM	**Featured Speaker:** Cost Effective and High Performance 28nm FPGA with New Disruptive Stack Silicon Interconnect (SSI) Technology *Woon-Seong Kwon, Xilinx Inc. (Suresh Ramalingam, Xin Wu, Liam Madden)*	**Featured Speaker:** Magnetic Field Imaging for Non-Destructive 3D Package Fault Isolation *Jan Gaudestad, Neocera (David Vallett)*	**Featured Speaker:** Determination of LTCC Shrinkage Variations from Tape Manufacturer to Consumer *James Kupferschmidt, Honeywell FM&T (Michael Girardi, Brent Duncan)*	**Featured Speaker:** Advancements in Phenomenological Understanding of Thinning and Planarization Processes for TSV-Enabled 2.5-3D Device Fabrications *Frank Wei, DISCO Corporation*	**Featured Speaker:** Zero Stress Die-Attach for Wide Band Gap Semiconductor Power Devices *Katsuaki Suganuma, ISIR, Osaka University (Jiu Jinting, Syunsuke Koga, Tohru Sugahara, Semin Park, Sungwon Park, Cholmin Oh, Shijo Nagao)*
2:30 PM –2:55 PM	Assembly and Scaling Challenges for 2.5D IC *Liang Wang, Invensas Corporation (Charles Woychik, Guilian Gao, Scott McGrath, Hong Shen, Andrew Cao, Helen Katske, Ellis Chau, Sitaram Arkalgud, Eric Tosaya)*	SEM-based X-Ray Tomography of Sub-Micrometer Defects in 3D Integration *David Laloum, CEA Leti (Frederic Lorut, Guillaume Audoit, Pierre Bleuet)*	Improved Fabrication of Micro Channels in LTCC Circuitry and MEMS using QPAC Polyalkylene Carbonates as a Sacrificial Structure *Peter Ferraro, Empower Materials (Sugianto Hanggodo)*	IMS (Injection Molded Solder) Technology with Liquid Photoresist for Ultra Fine Pitch Bumping *Toyohiro Aoki, IBM Japan, Ltd. (Kazushige Toriyama, Hiroyuki Mori, Yasumitsu Orii, Jae-woong Nah; Seiichirou Takahashi, Jun Mukawa, Kouichi Hasegawa, Shiro Kusumoto, Katsumi Inomata, JSR Corporation)*	A High-Temperature, Wide Bandgap Discrete Plastic Package *Chad O'Neal, Arkansas Power Electronics International (Richard Lollar, Brandon Passmore)*
3:00 PM –3:25 PM	Development of 3D System in Package with TSV Technology *Shota Miki, Shinko Electric Industries Co., Ltd.(Sumihiro Ichikawa, Masaki Sanada, Takaharu Yamano)*	Perfect Edge 3D™: Enabling Root-Cause Failure Analysis *Suzanne Costello, MCS Ltd (Stewart McCracken)*	Laser Ablation of Thin Films on LTCC *Michael Girardi, Honeywell FM&T (Ken Peterson, Paul Vianco)*	Process Control at Post-Saw for Low-K Wafers *Matt Wilson, Rudolph Technologies (Rajiv Roy, Frank Wei)*	DBC Switch Module for Management of Temperature and Noise in 160-W/in3 Power Assembly *Woochan Kim, Virginia Tech (Jongwon Shin, Khai D. T. Ngo)*

COFFEE BREAK IN EXHIBIT HALL (GRAND BALLROOM): 3:25 PM - 4:00 PM

IMAPS Cafés sponsored by:

Wednesday, October 15, 2014

	INTERPOSERS & 3D PACKAGING	MODELING, DESIGN, & TEST	MATERIALS & PROCESSES	ADVANCED PACKAGING INTERCONNECTS & ASSEMBLY	FUTURE OF PACKAGING
4:00 PM –4:25 PM	An Integrated FDC-centric Approach for Process Engineering in BEOL for Advanced Packaging - A Case Study in Die Singulation Process Optimization *Richard Beaver, Rudolph Technologies, Inc. (Frank Wei, DISCO Corporation)*	Failure Analysis of Discolored ENIG Pads in the Manufacturing Environment *Monika Marciniak , Crane Aerospace and Electronics (Michael Meagher)*	Reliability of High Frequency LTCC using Electroless Nickel Immersion Gold (ENIG) Plating Technology *Patricia Graddy, DuPont Electronics & Communications/ MCM (Allan Beikmohamadi)*	High Value Thin Wafer Support Technology for 3DIC *John Moore, Daetec, LLC (J. Pettit, A. Law, A. Brewer)*	The Design and Development of a 15 kV SiC Half-Bridge Multi-Chip Power Module for Medium Voltage Applications *Zach Cole, Arkansas Power Electronics International (Jennifer Stabach, Greg Falling, Peter Killeen, Ty McNutt, Brandon Passmore)*
4:30 PM –4:55 PM	High Density Organic Interposer with Fine Feature Size for Advanced Packaging Applications *Christian Romero, Samsung Electromechanics Co, Ltd (Jeongho Lee, Mijin Park, Seonhee Moon, Kyungseob Oh, Kyoungmoo Harr, Youngdo Kweon)*	A New Method for Testing Electrolytic Capacitors to Compare Life Expectancy *Steph Gulbrandsen, DfR Solutions (Joelle Arnold, Nick Kirsch, Greg Caswell)*	Thermal Design and Measurements of a Switch Matrix Module Based on LTCC Technology *Saqib Kaleem, Ilmenau University of Technology (Sven Rentsch, Dirk Stöpel, Jens Müller, and Matthias Hein)*	A Novel Thin Wafer Handling Technology to Enable Cost Effective Fabrication for Through Glass Via Interposer *Alvin Lee, Brewer Science, Inc. (Jay Su, Kim Arnold, Dongshun Bai; Bor Kai Wang, Leon Tsai, Aric Shorey, Corning Advanced Technology Center/ Corning Inc.; Wen-Wei Shen, Chun-Hsien Chien, Hsiang-Hung Chang, Jen-Chun Wang, EOL / ITRI)*	Sandwich Structured Power Module for High Temperature SiC Power Semiconductor Devices *Takeshi Anzai, R&D Partnership for Future Power Electronics Technology (Hiroshi Sato, Yoshinori Murakami, Shinji Sato, Hidekazu Tanisawa, Kohei Hiyama, Fumiki Kato, Hiroki Takahashi)*
5:00 PM –5:25 PM	Cost and Yield Comparison of Wafer-to-Wafer, Die-to-Wafer, and Die-to-Die Bonding *Amy Palesko, SavanSys Solutions, LLC (Chet Palesko)*		Improving Copper-Ceramic Bonding through Interface Engineering *Lim Ju Dy, Nanyang Technological University (Chen Zhong, Daniel Rhee Min Whoo, Leong Kam Chew)*	Hermetic Electrical Feedthroughs Based on the Diffusion of Platinum into Silicon *Linda Rudmann, Laboratory for Biomedical Microtechnology, BrainLinks-BrainTools Cluster of Excellence (ExC1086) (Juan S. Ordonez, Hans Zappe, Thomas Stieglitz)*	Interconnect and Packaging Techniques for System Integration of High Power Assemblies that Improve Assembly Efficiency and Design Flexibility *Joseph Lynch, Interplex Industries (Richard Schneider)*
5:30 PM –5:55 PM	Optical Characterization and Defect Inspection for 3D Stacked IC Technology *Jean-Philippe Piel, FOGALE Nanotech (Gilles Fresquet)*		Zero Meta-material Ferroelectric Phase Shifter Embedded Within LTCC *Hossam Tork, University of Idaho (Aicha Elshabini, Fred Barlow)*	Cost Comparison of Temporary Bond and Debond Methods For Thin Wafer Handling *Chet Palesko, SavanSys Solutions, LLC*	Packaging Development and Construction for Efficient Extreme Current Power Delivery *How Lin, i3 Electronics (Ed Tasillo, Subahu Desai)*

EXHIBIT HALL RECEPTION (GRAND BALLROOM): 6:00 PM - 7:30 PM

Thursday, October 16, 2014

6 Professional Development Courses (PDCs) available 8am-12pm – See Pages 23-26 for more information.

FUTURE OF PACKAGING KEYNOTES & PANEL DISCUSSION 8:00 AM - 12:00PM

8:00 AM –12:00 PM An entire morning of the conference dedicated to the Future of Packaging…

8:00 AM - 8:45 AM | KEYNOTE:
Advanced Integration and Packaging Technologies for Miniaturization of Medical Devices

Thanks to the introduction on the market of its revolutionary Silicon capacitor technology, Ipdia has been involved since its creation into many projects related to miniature medical devices, especially minimally invasive implantable devices.

This presentation will also briefly deal with advanced IC technologies but the emphasis will be put on other and complementary technologies such as Advanced Packaging and integration of new functions like passive components into semiconductor based technologies. It will show how these new technologies can help significantly reduce the volume of components and the devices which are using them.

Considerations on performances and reliability will be shared during this presentation: in particular the combination of low consumption (thanks to low leakage), stability and reliability. The semiconductor industry has been working now for years with reliable predictive models. We will show how these models can be used to select components, thanks to the fact that the real behavior of components and devices follows quite well the physics.

Finally, several relevant and illustrative examples of devices will be presented to conclude the presentation: heart, brain, nerves, eyes, ears...almost every part of the human body will be illustrated.

Dr. Franck Murray *is presently the CEO of IPDIA, a company that he started in June 2009. IPDIA is developing, manufacturing and selling Integrated Passive Devices.IPDIA is generating 20+ M$ of sales (with a yearly growth above 50%) and has 120 employees. Since its start, IPDIA has a worldwide commercial presence and sells 90% outside Europe.*

Franck got his Engineer Degree from Ecole Centrale de Paris in 1984 and an MBA at ESSEC (Paris) in 2003. He has also a PhD in Physics.

After his PhD, his first experience was with Philips in the development of LEDs. This first experience led him to create a start up in Material Analysis and then move to a position of CTO of a start up in the field of optical disk. He came back to Philips in 1996 (becoming NXP in 2006) to occupy various positions in Operations in Semiconductors Wafer Fab. He moved to Corporate Innovation and R&D in 2000 with the assignment to develop new technologies and design tools and find new ways to miniaturize electronic devices. He also occupied several technology related corporate positions. This led to the creation of advanced and original technologies to integrate passives devices into Silicon wafers. All this work has constituted the roots of today's IPDiA technologies.

8:45 AM - 9:30 AM | KEYNOTE:
Packaging Challenges for Wearable Devices

Wearable electronics is the next logical stage of computing from the current mobile one represented by phones and tablets. Wearable version is not merely a shrinking of current mobile devices, but also reimagining everything from fundamental use cases to user interactions. It would not be sufficient to make miniature phones on wrists or video projectors around heads and consider them the sum of wearable devices. With the intimate nature that is implied by wearable electronics, a complete rethinking on utility, ubiquity, and user behavior is needed. This covers many broad features such as health, identity, presence, notifications, etc.

To deliver the full wearable computing experience with new and tailored features, the hardware has to adapt significantly to be compatible with an individual's lifestyle. This means the wearable devices have to be small and light (miniaturized and low power electronics), rugged (water resistant and long lasting cosmetics), biocompatible (non-allergic and easily cleanable), possess intuitive user interface (control and feedback) and be stylish (unique and personal). This drives the whole product design, from chip packaging to system assembly.

The microelectronics packaging challenges for wearable devices are different from mobile devices in terms of components, performance, and reliability. The expected components include multiple sensor chips and their signal collectors such as windows, electrodes, etc., besides conventional digital and analog components. Due to extreme size and power limitations, packaging needs to be tuned to intelligent switching off and duty-cycling various sub-systems. This indicates that the packaging has to be done along with the device mechanical and cosmetic design to realize the functionality while meeting industrial design requirements. Reducing this integrated approach back to component level for defining the reliability tests becomes a challenge. Other aspects of product development such as test, yield, automation, and second sourcing also need to be developed. In conclusion, wearable devices provide unique opportunities and challenges to microelectronics packaging, and could potentially lead to new packaging, test and reliability standards.

Dr. Ilyas Mohammed *is a Senior Director of Wearable Products Design and Development at Jawbone. His team works on the wearable products such as the UP band that focus on health. He has done R&D work in the microelectronics packaging industry for 15 years. He has dozens of published papers and more than 50 issued US patents. He obtained his Ph.D. from The University of Texas at Austin and B.Tech. from the Indian Institute of Technology, Madras, India.*

Thursday, October 16, 2014

FUTURE OF PACKAGING KEYNOTES & PANEL DISCUSSION 8:00 AM - 12:00PM

8:00 AM –12:00 PM An entire morning of the conference dedicated to the Future of Packaging…

9:30 AM - 10:15 AM | KEYNOTE:
Stacked 3D Memory Technology – Challenges And Opportunity

The appetite for higher bandwidth and lower power are driving technologists and system architects to reconsider how processors and memory can work more efficiently and with improved proximity.

Hybrid Memory Cube (HMC) is a new memory architecture that enables significantly higher performance and lower energy per bit. HMC incorporates 3D Silicon integration with a stacked memory and controller in a single package incorporating heterogeneous multi die stacking with Through Silicon Vias.

Enabling this technology has required innovation and integration and solving several technical challenges. In this talk key enabling technologies and their challenges will be discussed.

The new 3D Memories such as Hybrid Memory Cube, Wide I/O 2, and High Bandwidth Memory provide opportunities for innovation in wafer and package technology for the future.

Kunal Parekh *started his career at Micron R&D in 1990. Over the past two decades, he has had positions of increasing responsibility, leading DRAM R&D Process Integration teams including the definition of advanced DRAM nodes, development and integration of FEOL, CMOS, BEOL and TSV. From 2011 to 2013, Kunal has successfully lead the development, qualification, yield ramp and production of 45nm 300mm Phase Change Memory (PCM). Currently Kunal leads the Advanced Packaging R&D group at Micron. Kunal has authored over 160 US patents and has served on the Symposium on VLSI Technology's Technical committee.*

10:15 AM - 10:30 AM: Coffee Break in Foyer
IMAPS Breaks sponsored by:

Invensas™

Legoland Balboa Park

Thursday, October 16, 2014

PANEL DISCUSSION 10:30 AM - 12:00PM

8:00 AM –12:00 PM An entire morning of the conference dedicated to the Future of Packaging…

"FUTURE OF PACKAGING"

Moderator: Subramanian "Subu" Iyer, IBM Fellow, Microelectronics Division, IBM Systems & Technology Group

Silicon is often credited with starting the modern electronics and IT age with the invention of the transistor and its subsequent miniaturization, but we often forget that packaging allowed these devices to be interconnected and actually become useful. With the relentless scaling of the transistor, on-chip interconnections took front stage and the System-on-Chip era took over and for most part packaging took back stage with the primary focus on cost reduction. In fact key pitches in the packaging and board areas have scaled only modestly by a factor 3-4 during the period that silicon features have scaled by over a factor of 1000.

However, with silicon scaling sputtering to a halt, is this image of packaging as Silicon's poor cousin poised for a big change? How will packaging pick up the slack? Will packaging executives seize the opportunity and begin this transformation by investing along the same lines as silicon has been. Or will Silicon foundries expand into adjacent spaces and make the whole argument moot? How will packaging uniquely add to new value to the new trends such as the Internet of things, medical electronics, wearable electronics, transportation electronics, lighting and such? Or is the premise that packaging in the last several years has been stagnant not quite true?

This panel, made up of industry and academic stalwarts in the field, and moderated by Subu Iyer, IBM Fellow and Director of System Scale Integration at IBM, will debate these issues. How does packaging need to change to enable the next revolution in electronics, and how do we think it will change our lives and the way we do things. Will we willingly embrace and lead this change? Will we invest in our future or is it better for foundries with their larger capital budgets, to take over relevant packaging functions and make these changes happen?

Panelists:

Steve Bezuk *is Senior Director of IC Package Engineering at Qualcomm. Steve's group is responsible for current and future generations of packaging technologies for all of Qualcomm's wireless applications. Prior to joining Qualcomm Steve was with Kyocera, Unisys, Sperry-Univac and RCA's Sarnoff Research Center. Steve has worked and managed groups in a variety of areas, including of amorphous silicon research, CMOS, Bipolar and GaAs IC process development, Laser enhanced materials processing, and wirebond, TAB, Flip Chip, MEMS, and TSV packaging.*

Steve is also very active in the IEEE CPMT and is their current VP of Technology. Steve is also active with the ECTC Conference for the society and was the General Chair for the 2004 ECTC conference and is the Current Publications Chair.

Steve has a B.S. in Chemistry from the University of Pittsburgh and a Ph.D. in Chemistry from the University of Minnesota.

Ilyas Mohammed *is a Senior Director of Wearable Products Design and Development at Jawbone. His team works on the wearable products such as the UP band that focus on health. He has done R&D work in the microelectronics packaging industry for 15 years. He has dozens of published papers and more than 50 issued US patents. He obtained his Ph.D. from The University of Texas at Austin and B.Tech. from the Indian Institute of Technology, Madras, India.*

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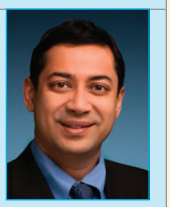

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Panelists continued on next page

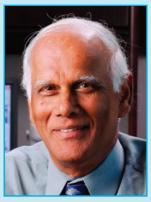
Thursday, October 16, 2014

PANEL DISCUSSION 10:30 AM - 12:00PM

Bharath Rangarajan *is the President of Advanced Nanotechnology Solutions Inc. (ANS Inc). With over 20 years of experience in the semiconductor space, and having held senior management positions at AMD, Bharath is one of the leading strategists in the technology sector, with a strong background and experience in technology, manufacturing, marketing, strategy and business development. Bharath has been responsible for creating and executing some game-changing moves including large acquisitions and divestitures that enabled AMD's transformation into technology-leader and volume microprocessor solutions provider. These moves include the spin off of AMD's memory business into Spansion, the antitrust litigation and settlement with Intel, and the acquisition of ATI.*

His strategies and transactions enabled the creation of GLOBALFOUNDRIES (GF), a powerhouse in the capital-intensive semiconductor-manufacturing segment, right in the middle of the financial crisis. This strategy fundamentally changed AMD, dramatically improved its free cash flow and shored up the balance sheet. As part of this transaction, GF built a state of the art fab in Malta, NY. A visionary, with a strong sense for business fundamentals, Bharath's passion is to create value through growth. Bharath is a strong believer in differentiation and innovation and is passionate about bringing jobs to the US.

Bharath holds bachelor's degree in Chemical Engineering from the Indian Institute of Technology at Delhi, a doctorate in Chemical Engineering from Michigan State University, and an MBA from the University of California at Berkeley.



Prof. Rao Tummala *is a Distinguished and Endowed Chair Professor, and Founding Director of NSF ERC at Georgia Tech, pioneering Moore's Law for System Integration. Prior to joining Georgia Tech, he was an IBM Fellow, pioneering the first plasma display and multichip electronics for mainframes and servers.*

He has received many industry, academic and professional society awards including Industry Week's award for improving U.S. competitiveness, IEEE's David Sarnoff, IMAPS' Dan Hughes, Engineering Materials from ASM, Total Excellence in Manufacturing from SME. He received Distinguished Alumni Awards from University of Illinois, Indian Institute of Science and Georgia Tech. In 2011, Prof. Tummala received the Technovisionary Award from Indian Semiconductor Association and IEEE Field Award for contributions in electronics systems integration, and cross-disciplinary education. He received his BS from Indian Institute of Science, and Ph.D. from University of Illinois.

Prof. Tummala has published about 500 technical papers, holds 74 patents and inventions; authored the first modern Microelectronics Packaging Handbook, the first undergrad textbook Fundamentals of Microsystems Packaging, and the first book introducing the System-On-Package technology. He is a Fellow of IEEE, a member of National Academy of Engineering as well as past President of IEEE-CPMT and the IMAPS Societies.

12:00 PM - 1:00 PM: Lunch Break (Attendees on their own for lunch)

Midway Museum

Thursday, October 16, 2014

	INTERPOSERS & 3D PACKAGING	MODELING, DESIGN, & TEST	MATERIALS & PROCESSES	ADVANCED PACKAGING INTERCONNECTS & ASSEMBLY	FUTURE OF PACKAGING
1:00 PM –4:10 PM	**Advanced Interconnect Innovations** *Chairs: Jeffrey Hartman, Northrop Grumman; Josh Luff, Honeywell* This session will explore applications and processes for integration and interconnect technologies.	**RF, MM/Microwave Applications** *Chairs: Ken Kuang, Torrey Hills Tech; Hassan Hashemi, Newport Media* RF and microwave applications present complex packaging challenges driven by tight electrical design and process challenges. Demanding mechanical reliability requirements determined by end application place further constraints on cost-size-reliable-and repeatable interconnect and packaging solutions for this class of products. This session brings together a wide range of papers on various microwave application including packaging for automotive, MM wave antenna, passive integration, and cooling ideas for III-V material used in such applications.	**Bonding Materials and Processes** *Chairs: Maria Durham, Indium Corp.; Ganesh Krishnan, Formfactor Inc.; Li Jiang, Texas Instruments* Bonding materials and processes for TSV and wirebonding.	**Photonic Packaging** *Chairs: John Mazurowski, Penn State Electro-Optics Center; Vivek Raghunathan, Intel Corporation* Photonics Packaging encompasses all aspects of packaging but also light manipulation at the device-package coupling interface and inside the package. The photons in this case can either act as data transmitters in case of optical computation and communication (e.g. Fiber optic cables, optical filters, optical waveguides, optical modulators) or as optical power source in case of lasers, LEDs etc.	**Printed Electronics & Additive Manufacturing** *Chairs: Mike Newton, Newton Cyberfacturing; Samson Shahbazi, Heraeus Electronic Materials Division* This session is focused on 2D and 3D digital manufacturing, printed electronics and additive manufacturing as an emerging electronic packaging technology. Presentations are on the latest materials, process, design & emerging applications of printed electronics and printed circuit structural technology.
1:00 PM –1:25 PM	**Featured Speaker:** Adhesion Interface Study of PMV (Plating Mold Via) Interconnection in Double Side Molded Packaging Module *DoJae Yoo, Samsung Electro Mechanics. Co (Jong-In Ryu, Jae-Hyun Lim, Gyu-Hwan Oh, Jin-Su Kim, Eun-Jung Lim, Yong-Choon Park, Young-Nam Hwang, Il-Hyeong Lee, Tae-Sung Kang)*	**Featured Speaker:** A New Approach for Reliable and Compact 3D Integration of mmW Transceivers on Silicon Using High-Impedance Surface Antennas *Ossama El Bouayadi, CEA-LETI (Yann Lamy, Laurent Dussopt)*	**Featured Speaker:** The Effect of Plating, Surface Finish, Bond Line Thickness and Thermal Treatment on AuSn Solder Joints *Greg Rudd, Spectra-Mat, Inc (John Paff, Rob Brox)*	**Featured Speaker:** Photonic Interconnects for Data Centers *Tolga Tekin, Fraunhofer IZM (Nikos Pleros, CERTH/ITI; Dimitris Apostolopoulos, National Technical University of Athens)*	**Featured Speaker:** 3D Micro Dispensing & Photonic Curing of Silver Nanoinks on Low Thermal Stability Molded Plastic Parts *Michael Mastropietro, Novacentrix (Ken Church, Xudong Chen, Vahid Akhavan, Ian Rawson)*
1:30 PM –1:55 PM	High Productivity Thermo-Compression Flip Chip Bonding *Bob Chylak, Kulicke and Soffa Industries, Inc. (Tom Colosimo, Matthew Wasserman, Michael Schmidt-Lange, Horst Clauberg, Patrick Desjardins)*	Substrate-Integrated Divider Networks in LTCC with Optimized Tolerance / Isolation Properties for Ka-band Satellite Systems *Tobias Klein, IMST GmbH (Peter Uhlig, Carsten Günner, Reinhard Kulke)*	Novel Temporary Wafer Bonding Materials for Very-High- Temperature Processing *Michelle Fowler, Brewer Science, Inc. (Dongshun Bai, Gu Xu)*	A Decade of High Accuracy Die Attach Equipment and Process Developments (Addressing Photonics Device Packaging Challenges) *David Halk, AMICRA Microtechnologies Inc.*	Investigation of Rapid-Prototyping Methods for 3D Printed Power Electronic Module Development *Haotao Ke, North Carolina State University (Adam Morgan, Ronald Aman, Douglas Hopkins)*
2:00 PM –2:25 PM	Design and Direct Assembly of 2.5D/3D Rigid Silicon Interposer on PCB *Farhang Yazdani, BroadPak Corporation*	Qualification of RF-IC Package for Automotive Applications *Mumtaz Bora, Peregrine Semiconductor*	Partitioning Responses of a Thermoplastic Temporary Bonding Material in a Thermal Compression Bonder *Juni Myers, Brewer Science, Inc.*	Can GaN Based Light Emitting Diodes with Backside Reflectors Improve the Optical Output? *Gunwoo Kim, University of California, Irvine (Yu-Chou Shih, Frank Shi)*	Direct Write Electronics - Thick Films on LTCC *Tim Eastman, Honeywell FM&T (Adam Cook)*

COFFEE BREAK IN FOYER: 2:25 PM - 2:45 PM

IMAPS Cafés sponsored by:

Thursday, October 16, 2014

	INTERPOSERS & 3D PACKAGING	MODELING, DESIGN, & TEST	MATERIALS & PROCESSES	ADVANCED PACKAGING INTERCONNECTS & ASSEMBLY	FUTURE OF PACKAGING
2:45 PM –3:10 PM	Development of Stress Compensation Layer for Thin Pixel Modules 3D Assembly *Gabriel Pares, CEA-Leti (T. McMullen, S. Tomé, L. Vignoud, R. Bates, C. Buttar)*	Capacitive-Based, Closed-Loop Frequency Control of Substrate-Integrated Cavity Filters *Shahrokh Saeedi, University of Oklahoma (William Wilson, Tyler Ashley, Hjalti Sigmarsson)*	Microstructure Analysis of Heavy Aluminum and Copper Wire During Bonding Process *Florian Eacock, University of Paderborn (Thomas Niendorf, Simon Althoff, Mirko Schaper; Karsten Guth, Infineon Technologies)*	Silver Plating for LED Applications Technology, Processes and Production Experience *Steven Burling, Metalor Technologies (UK) Ltd (Gary Nicholls, Metalor USA; Peter Christensen, Metalor Technologies, China; Sadayuki Nagatomo, Kazuhiko Shiokawa, Metalor Technologies, Japan)*	Measurement of Electrical Resistivity of Direct Digital Printed Conductive Traces Using Near-Field Microwave Microscopy *Maria Cordoba-Erazo, University of South Florida (Eduardo Rojas-Nastrucci, Thomas Weller)*
3:15 PM –3:40 PM	Short Loop Electrical and Reliability Learning for TSV-Mid Wafer Front-Side Processes *Klaus Hummler, SEMATECH (Tyler Barbera, Kai-Hung Yu, Shan Hu, Akira Fujita, Fred Wafula, Gyanaranjan Pattanaik, Alison Gracias, Victor Vartanian, Steve Olson, Larry Smith, Jack Enloe, Gert Leusink, Kenneth Matthews, Kaoru Maekawa, Brian Sapp)*	Influence of Fabrication Process Parameters and Material Properties on Process Yield Performance of RF and Microwave Thin Film Based Termination Resistor *Akhlaq Rahman, Thin Film Technology Corporation (Mike Howieson)*	Reliability Study of Silver, Copper and Gold Wire Bonding on IC Device *Hongtao Gao, Alpha & Omega Semiconductor Co., Ltd (Jun Lu, Richard Lu, Wei Xin, Xiaojing Xu)*	Silver Paste with Nano-sized Glass Frits for Silicon Solar Cells *Yu-Chou Shih, University of California, Irvine (Yue Shao, Yeong-Her Lin, Frank Shi)*	Photopatternable Laminate Dielectric *Corey O'Connor, Dow Electronic Materials (Robert Barr, Jeff Calvert, Mike Gallagher, Elissei Lagodkine, Joon Seok Oh, Andy Politis)*
3:45 PM –4:10 PM	A Case Study of the Reliability of Copper Bond Wires In Plastic Encapsulated Integrated Circuits *Ken Turner, Hi-Rel Laboratories*	TL MIM CAPs: Transmission Line Metal-Insulator-Metal Capacitors in High Frequency Hybrid Modules *Cenk Atalan, ASELSAN A.S.*	Analysis Method of Tool Topography Change and Identification of Wear Indicators for Heavy Copper Wire Wedge Bonding *Paul Eichwald, University of Paderborn (Walter Sextro, Simon Althoff, Florian Eacock, Andreas Unger, Karsten Guth)*	High-brightness LEDs of Big Chip Size Packaged on Thru-Ceramic Via with Optimized Thermal Dissipation and Optical Performance *Liang Wang, Invensas Corporation (Gabe Guevara, Grant Villavicencio, Roseann Alatorre, Hala Shaba, Rey Co, Ellis Chau, Eric Tosaya)*	

NATEL

We make amazing things happen.™

Natel's Second Annual Supplier of the Year Awards

Based on the success of last years awards, NATEL EMS will again recognize its best supplier's Monday evening with its Natel supplier of the Year awards during IMAPS 47th annual International Symposium. The awards presentation will be held at the Town Country Resort and Conference Center in San Diego, CA during the Welcome Reception, Monday, October 13, 2014."The Supplier of the Year" award winners represents a partnership, dedication and commitment to consistently perform above expectations. This continues to play an important role in Natel's success," said Sudesh Arora, President of Natel EMS. " We appreciate the efforts of these suppliers and look forward to a mutually beneficial continued relationship in the future."The awards recognize the significant contributions of Natel suppliers as part of the company's product and performance achievement. The winners represent Natel's view, as the best the microelectronics/electronics industry has to offer in innovative technology, superior quality, outstanding launch support, crisis management and competitive total enterprise cost solutions. The suppliers of the Year winners are chosen by the Natel team of purchasing, engineering, quality, manufacturing and logistics executives.

Microelectronics Foundation Golf Invitational

Monday, October 13, 2014

Riverwalk Golf Course 1150 Fashion Valley Road, San Diego, CA 92108
www.riverwalkgc.com

The Riverwalk Golf Course encompasses three nine-hole layouts that can be combined in a variety of ways to create a unique experience every time you play. Distinctive in character but consistent in quality, every hole was meticulously designed by Ted Robinson, Sr. and Jr. in the old style, leaving the terrain completely natural. Mature stands of palm, oak and eucalyptus trees frame undulating fairways and manicured greens, with numerous wetland areas, nearly 100 bunkers and an array of picturesque water features creating both strategic diversity and a visually stunning backdrop for golf.

Cost: $125 per person — $450/four-some

The cost includes: Transportation to and from the course, greens/cart fees, shotgun start, and a breakfast/lunch — TBD.

All proceeds from this event will benefit the IMAPS Microelectronics Foundation.

Special Awards and Activities tentatively planned:

Closest to the Pins • Longest Drives • Team Awards

Golfers will tee off shortly after arriving at the course. Times are tentative and will be confirmed before the outing. Callaway rental clubs are available for $50 plus tax.

Riverwalk Golf Course

8:00 am Shotgun Start – "Best Ball" Scramble

All proceeds from this event will benefit the IMAPS Microelectronics Foundation.

REGISTER FOR GOLF ONLINE at www.imaps2014.org

GOLF FEES ON PAGE 2 UNDER "SESSIONS" DURING CHECK-OUT

About the IMAPS Microelectronic Foundation

Mission Statement:
The Foundation's role is to support student activities related to the study of Microelectronic Packaging, Interconnect and Assembly.

Foundation Chair:: David Virissimo, Coining Inc • Golf Co-Chair: Vern Stygar, Asahi Glass

Sponsorship Opportunities:

Eagle Sponsor - $3,000

- Company logo/name displayed as Awards Reception Sponsor and Putting Contest Sponsor.
- Entrance of two four-somes.
- Additional three hole sponsorships with signage.
- Company logo/name on all event promotional signs, materials and website.
- Company may provide take-away products to be handed to all golfers. Golf-related items usually most appropriate (e.g., golf towels, balls, tees, etc.). At expense of sponsor.

Birdie Sponsor - $1,500

- Company logo/name displayed at Breakfast/Registration
- Entrance of one four-some.
- Includes one hole sponsorship with signage.
- Company logo/name on all event promotional signs, materials and website.

Hole Sponsor - $500 / $750

- Sponsorship of one hole with signage.
- Entrance of one golfer ($500) or one 4-some ($750).
- Company logo/name on promotional materials and website

2014 Student Symposium Programs

Honeywell

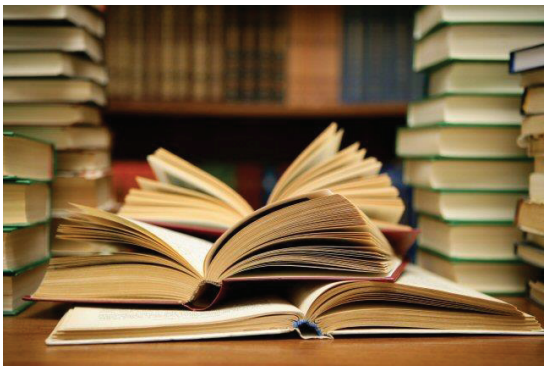
Honeywell is the sole sponsor proudly supporting all IMAPS 2014 students and related activities during the 47th Symposium.

STUDENT OPPORTUNITIES AT *IMAPS 2014 – SAN DIEGO*

*The **International Microelectronics Assembly and Packaging Society (IMAPS)** is the largest society dedicated to the advancement and growth of microelectronics and electronics packaging. The 47th International Symposium on Microelectronics will take place in San Diego, CA, from Oct. 14-16 2014. The IMAPS Technical Committee seeks original papers that present progress on technologies throughout the entire microelectronics/packaging supply chain. All papers are PEER-REVIEWED and will also be considered for IMAPS Journal. For more Information please visit www.imaps2014.org*

EDUCATION

- Learn from the industry's best
- Short Courses (PDCs) by Experts
- Access to hundreds of cutting-edge papers in the symposium *Proceedings*
- Access to *International Journal of Microelectronics and Electronic Packaging*
- *Advancing Microelectronics* Magazine



CAREER OPPORTUNITIES

- Speaking Opportunities for Students
- ***PUBLISH!*** Peer-review of all papers and consideration for IMAPS *Journal of Microelectronics and Electronic Packaging*
- Get Noticed! ***Volunteer*** to lead a Session
- Networking with Global Industry Leaders
- Seek Internships/Jobs at Meetings
- IMAPS Website & JOBS Marketplace

REWARDING

- The ***Microelectronics Foundation*** sponsors Student Paper Competitions and Awards in conjunction with IMAPS 2014 that are generously sponsored by HONEYWELL:

$1000 (Best), $500 (3-Outstanding), $500 (Best Posters), $500 (Best Booths)

- Student Travel Stipends to Attend Conferences
- Attend = Automatic 1-yr. Student Membership
- Volunteer opportunities look great on resumes!

For more Information, please contact Brian Schieman, IMAPS: bschieman@imaps.org

Things to Do in San Diego

Visitors to San Diego have a dazzling array of choices to make. Between the natural beauty of the beaches, parks, countless shopping and dining options, and a bustling nightlife, there's a world of possibilities.

Take Advantage of "All that Water"

Depending on your skill level and the size of your party, you can rent anything from a single or double kayak or a people-powered paddle boat to a fast-moving sailboard, personal watercraft, or sailboat at one of the many boat rental places in and around Mission Bay. Several of the larger hotels, including the Bahia, the Catamaran, and Paradise Point, have rental facilities, as do the Mission Bay Sports Center at Santa Clara Point and Seaforth Boat Rental at Quivira Basin. Be sure to bring along some bottled water and plenty of sunscreen; San Diego sunlight can be intense year-round.

The San Diego Zoo

With approximately 4,000 animals on more than 100 lushly-planted acres, the best way to get your bearings is with a narrated tour on a double-decker bus. Your ticket is also good for an express bus that makes stops throughout the Zoo, so you can hop on and off at various points. Another great idea: an aerial tram ride providing a fantastic overview of the entire area. In addition to the Zoo's famous pandas, on loan from the People's Republic of China, top exhibits include the Polar Bear Plunge and Hippo Beach (both enclosures offer underwater vantage points); the brand new Monkey Trails exhibit, home to many endangered species; and the tropical jungle environs of Tiger River. www.sandiegozoo.org.

Sea World

Just about everyone has heard of Sea World and its famous killer whales. And while the Shamu shows remain popular with fans of all ages, the park has plenty more to offer. One of the best ways to experience Sea World is with a one-hour, behind-the-scenes tour that gives you a VIP view of animal housing and training facilities and research areas. (Other personalized tours are available as well. See Web site for details; tours should be booked in advance.) Then, be sure to check out favorite attractions like the delightful Penguin Encounter; Forbidden Reef, home to gentle bay rays you can touch and feed; Shark Encounter, where a walk-through, Plexiglas tube takes you into the midst of hundreds of sharks; and dozens of other exhibits and shows. Dining options range from snacks and fast food to sit-down restaurants. www.seaworld.com

Coronado Island

The island (actually, a peninsula) of Coronado is the location of one of the nation's loveliest beaches. Named one of the top 10 in America by the Travel Channel, Coronado Beach is family-friendly and well-patrolled by lifeguards. Here, you can swim, play volleyball, build a sandcastle, or simply relax. The most popular stretch of sand is known as Central Beach, adjacent to the historic Hotel Del Coronado. Constructed in 1888, the charming red-roofed hotel has hosted numerous presidents and celebrities. To the north, the beach offers a designated area where dog owners can let their pets romp in the surf, while to the south, the Shores area is a popular spot for bodyboarding.

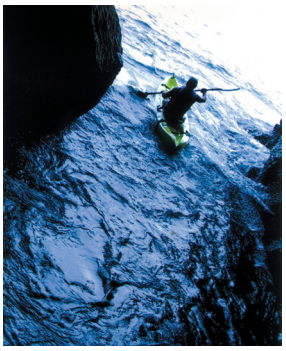
Downtown San Diego – A Little Bit of Everything

Depending on your interests, you can sightsee, shop, stroll, see a movie, dine, or dance into the night. Your first stop should be Horton Plaza, a multi-story, open air mall known for its eclectic architecture, people-watching opportunities and more than 100 stores and shops. Make a purchase here and you'll get three free hours of parking - ample time for shopping and for exploring the surrounding Gaslamp Quarter. Home to art galleries, boutiques, coffeehouses, neighborhood bars, swanky nightclubs and restaurants of every stripe, the Gaslamp Quarter offers something for every budget. Dining options range from family-style restaurants and chains to upscale steakhouses, Italian trattorias, tapas bars and Asian eateries. Several clubs and restaurants host live music (the House of Blues has a branch here) while others feature DJs, televised sports, or simply the buzz of lively conversations. Movie theaters include the Gaslamp Stadium 15 and the UA Horton Plaza; and if it's baseball season, you can catch a Padres game at the spectacular Petco Park.

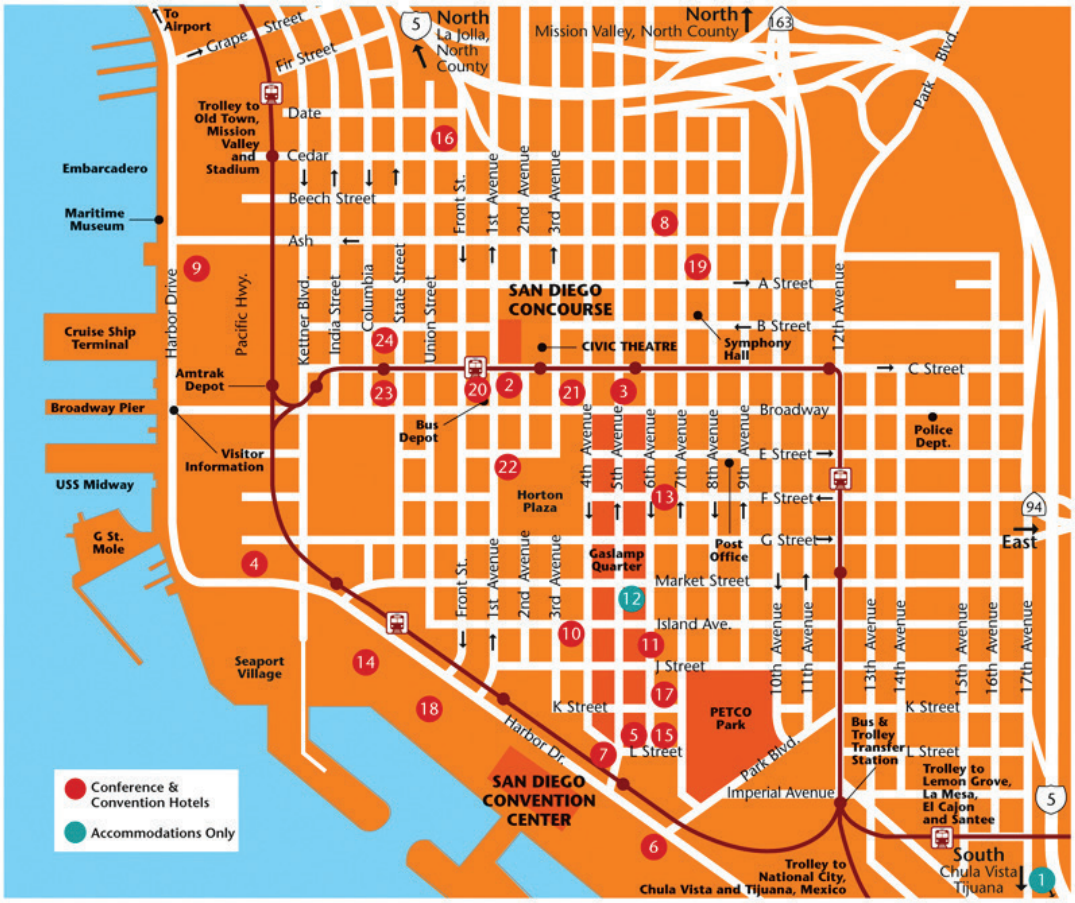
Dining on the Water

A real treat is to have dinner at one of the restaurants right on the boardwalk facing the ocean in Mission or Pacific Beach. After dinner, walk north or south along the boardwalk to catch the flavor of these seaside neighborhoods.

Take a cruise on the Mississippi-style sternwheeler Bahia Belle, which shuttles between two hotels on Mission Bay. The views are fabulous from all three decks, and the bay has a quiet beauty all its own at night. Cruises from 6:30 p.m. to 9 p.m. are designated Family Hours, while those from 9:30 p.m. on are for the 21 and up crowd only. Catch the boat at the Bahia Hotel and enjoy a short tour before stopping at the Catamaran Hotel. After a brief stop, the ship returns to the Bahia.



San Diego Area Map



Downtown/Balboa Park/Hillcrest/North Park Accommodations

Map Location	Hotel	Guest Rooms
1	America's Best Value Inn – Convention Center	42
2	The Bristol San Diego	102
3	Courtyard by Marriott San Diego Downtown	245
4	Embassy Suites Hotel San Diego Bay – Downtown	337
5	Hard Rock Hotel San Diego	420
6	Hilton San Diego Convention Center	1,190
7	Hilton San Diego Gaslamp Quarter	282
8	Holiday Inn Express – Downtown San Diego	136
9	Holiday Inn on the Bay	600
10	Horton Grand Hotel	132
11	Hotel Solamar San Diego	235
12	Hostelling International	33
13	Ivy Hotel	142
14	Manchester Grand Hyatt San Diego	1,625
15	Omni San Diego Hotel	511
16	Radisson Hotel Harbor View	333
17	San Diego Marriott Gaslamp Quarter	306
18	San Diego Marriott Hotel & Marina	1,362
19	Sheraton Suites San Diego at Symphony Hall	264
20	The Sofia Hotel	212
21	The US Grant	270
22	The Westin Horton Plaza San Diego	450
23	The Westin San Diego	436
24	W San Diego	258

San Diego Climate

Temperatures

Average monthly temperatures range from 57.3 °F (14.1 °C) in January to 72.5 °F (22.5 °C) in August, although late summer and early autumn are typically the hottest times of the year with temperatures occasionally reaching 90 °F (32 °C) or higher. Snow and ice are rare in the wintertime, typically occurring only inland from the coast when present. "May gray and June gloom," a local saying, refers to the way in which San Diego sometimes has trouble shaking off the fog that comes in during those months. Temperatures soar to very high readings only on rare occasions, chiefly when easterly winds bring hot, dry air from the inland deserts (these winds are called "Santa Ana winds").

The record high temperature at the National Weather Service office in San Diego of 111 °F (44 °C) was on September 26, 1963. The record low temperature was 25 °F (−4 °C) on January 7, 1913.

Precipitation

San Diego has on average 146 sunny days and 117 partly cloudy days a year. The average annual precipitation is less than 12 inches (300 mm), resulting in a borderline arid climate. Rainfall is strongly concentrated in the cooler half of the year, particularly the months December through March, although precipitation is lower than any other part of the U.S. west coast. The summer months are virtually rainless. Rainfall is highly variable from year to year and from month to month, and San Diego is subject to both droughts and floods. Hurricanes and thunderstorms are very rare. Coastal areas are driest; Cleveland National Forest receives more precipitation, and some inland areas like Laguna Mountains average more than 30 inches of rainfall per year.

At the National Weather Service office, there are an average of 43 days with measurable precipitation. The wettest year was 1941 with 24.93 inches (63.3 cm) and the driest year was 1953 with 3.23 inches (8.2 cm). The most rainfall in one month was 9.09 inches (23.1 cm) in January 1993. The most rainfall in 24 hours was 3.23 inches (8.2 cm) on April 5, 1926.

Variation

Climate in the San Diego area often varies dramatically over short geographical distances, due to the city's topography (the Bay, and the numerous hills, mountains, and canyons), thus exhibiting microclimate: frequently, particularly during the "May gray / June gloom" period, a thick "marine layer" cloud cover will keep the air cool and damp within a few miles of the coast, but will yield to bright cloudless sunshine between about 5 and 15 miles inland—the cities of El Cajon and Santee for example, rarely experience the cloud cover.

History of San Diego

Pre-Colonial and Colonial Period

The area has long been inhabited by the Kumeyaay Native American people. The first European to visit the region was Juan Rodríguez Cabrillo. Cabrillo was Portuguese (his name in Portuguese was Joao Rodrigues Cabrilho) but he was a long-term resident of Spanish America. He was commissioned by Viceroy Antonio de Mendoza to continue the explorations of California. In 1542, Cabrillo discovered San Diego Bay, which he named San Miguel. He went ashore, probably in the Ballast Point area of Point Loma. His landing is re-enacted every year at the Cabrillo Festival sponsored by Cabrillo National Monument.

The bay and the area of present-day San Diego were given their current name sixty years later by Sebastián Vizcaíno when he was mapping the coastline of Alta California for Spain in 1602. The explorers camped near a Native American village called Nipaguay and celebrated mass in honor of San Diego de Alcala (Saint Didacus of Alcalá). California was then part of the Viceroyalty of New Spain under the Audiencia of Guadalajara.

In May 1602, Vizcaíno left Mexico and beat his way north with two small ships, the San Diego and the Santa Tomas. By November of that year, his ships were anchored in the lee of Point Loma. Markedly different from the conquistadors, Vizcaíno had no experience commanding an expedition or conquering rich tribes. Instead, he was a merchant who hoped to establish prosperous colonies. After holding the first Catholic service conducted on California soil on the feast day of San Diego de Alcala (also the patron saint of his flagship), he renamed the bay. When he left after 10 days anchored there, he was enthusiastic about its safe harbor, friendly natives, and promising potential as a successful colony. After a difficult voyage north during which 40 of his crew died, Vizcaíno returned to Mexico, still convinced that San Diego would be the perfect location for a Spanish colony. Despite his enthusiasm, the Spanish were unconvinced, lured, instead, to spend resources seeking the rich trading opportunities in Asia. It would be another 167 years before California gained enough strategic value to generate colonization. When this time arrived, it was San Diego that was selected as Spain's first California settlement.

In 1769, Gaspar de Portolà and his expedition founded the Presidio of San Diego (military post), and on July 16, Franciscan friars Junípero Serra, Juan Viscaino and Fernando Parron raised and 'blessed a cross,' establishing the first mission in upper Las Californias, Mission San Diego de Alcala. Colonists began arriving in 1774. In the following year the Kumeyaay indigenous people rebelled against the Spanish. They killed the priest and two others, and burned the mission. Father Serra organized the rebuilding, and two years later a fire-proof adobe and tile-roofed structure was built. By 1797 the mission had become the largest in California, with a population of more than 1,400 presumably converted Native American "Mission Indians" relocated to and associated with it.

Mexican Period

In 1821 Mexico won victory over the Spanish Empire in the Mexican War for Independence. The Mexican Province of Alta California was created. The San Diego Mission was secularized in 1834, and 432 people petitioned Governor José Figueroa to form a pueblo. Commandant Santiago Arguello endorsed it. Juan María Osuna was elected the first alcalde ('mayor'), winning over Pío Pico in the 13 ballots cast. Beyond town Mexican land grants expanded the number of California Ranchos that modestly added to the local economy.

The original town of San Diego was located at the foot of Presidio Hill, in the area which is now Old Town San Diego State Historic Park. The location was not ideal, being several miles away from navigable water. Imported goods and exports (primarily tallow and hides) had to be carried over the La Playa Trail to the anchorages in Point Loma. This arrangement was suitable only for a very small town. In 1830 the population was about 600; in 1838 the town lost its pueblo status because of its dwindling population, estimated as 100 to 150 residents.

Joining the United States

Alta California became part of the United States in 1850 following the U.S. victory in the Mexican-American War and the Treaty of Guadalupe Hidalgo. San Diego, still little more than a village, was incorporated as a city and was named the county seat of the newly established San Diego County. The United States Census reported the population of the town as 650 in 1850 and 731 in 1860.

Although an estimated 10,000 stopped briefly in San Diego on their way to the San Francisco gold fields, few stayed, and San Diego remained sparsely settled during much of the 1850s. Despite its small population, this decade brought investors who saw the potential of San Diego. They bought lots, built rough homes and shops, and hoped. One, William Heath Davis, had such confidence that he spent $60,000 constructing a wharf near the property he had purchased near the foot of today's Market Street. Remembered as 'Davis' Folly,' it was completed by August 1851, but was seldom used. Clearly a financial

disaster, it received its death blow when, in 1853, the steamer Los Angeles crashed into it. The damage was never repaired. It had become clear that it was not worth fixing – in addition to it being largely unused, it had been so poorly built that the brittle piles kept snapping off. Davis tried and tried unsuccessfully to sell it. Finally, in 1862, the Army destroyed it, using timbers for firewood.

The failure of the wharf was an indication of depressed times. Frightened San Diego promoters watched and worried as houses were dismantled and shipped to more promising settlements. By 1860, many of the enterprises that had been established during the early 1850s had closed. The few businesses that survived suffered from water shortages, high costs of shipping, and a declining population. Only those visionaries who were convinced of San Diego's destiny stayed; most packed up and left. Those who stayed wondered when prosperity would make their lives brighter. Luckily, they did not have long to wait.

Fifty-three-year-old Alonzo Horton, a visionary San Diego needed, disembarked from the Orizaba on April 15, 1867. Although his first view was of barren, mesquite-covered land with a few decaying structures, he was awed, saying, "I have been nearly all over the world and it seemed to me to be the best spot for building a city I ever saw." He was convinced that the town needed a location nearer the water to improve trade. Unfaltering in his enthusiasm, less than a month after his arrival, he had purchased more than 900 acres of today's downtown for only $265, an average of 27.5 cents an acre. With boundless energy, he began promoting San Diego by enticing entrepreneurs and residents alike. He built a wharf and began to promote development there. The area was referred to as New Town or the Horton Addition. Despite opposition from the residents of the original settlement, which became known as 'Old Town,' businesses and residents flocked to New Town and San Diego experienced the first of its many real estate booms. In 1871, government records were moved to a new county courthouse in New Town, and by the 1880s New Town (or downtown) had totally eclipsed Old Town as the heart of the growing city.

Consolidation as an Urban Center

Military Presence

Significant U.S. Navy presence began in 1901, with the establishment of the Navy Coaling Station in Point Loma, and expanded greatly during the 1920s. Camp Kearny was established in 1917, closed in 1920, later reopened, and eventually became the site of Marine Corps Air Station Miramar. Naval Base San Diego was established in 1922, as was the San Diego Naval Hospital. The Marine Corps Recruit Depot San Diego was commissioned in 1921 and the San Diego Naval Training Center in 1923. (The Naval Training Center was closed on April 30, 1997.)

World's Fairs

San Diego hosted two World's Fairs, the Panama-California Exposition in 1915, and the California Pacific International Exposition in 1935. The expositions left a lasting legacy in the form of Balboa Park, the San Diego Zoo, and popularizing Mission Revival Style and Spanish Colonial Revival Style architecture locally and in Southern California as a regional aesthetic, and influencing design in the nation.

Modern San Diego

Since World War II, the military has played a leading role in the local economy. Following the end of the Cold War the military presence diminished considerably. San Diego has since become a center of the emerging biotech industry and is home to telecommunications giant Qualcomm.

San Diego's Town and Country Resort
IMAPS 2014

New Guest Rooms
New State-of-the-Art Wi-Fi
Same Award-Winning Service

- All Premium Royal Palm Tower Rooms have been reserved for IMAPS. These rooms are all newly renovated with New Décor from Floor to Ceiling, Bedding and HDTV's
- 2 New Wi-Fi Systems: The All-New "Meraki" Wi-Fi System in all Meeting Areas and the New AT&T State-of-the-Art System in all Guest Rooms

- Acres of Lushly Landscaped Gardens throughout the property
- 4 Restaurants, 2 Lounges, 3 Pools and Whirlpool
- 14,000 sq. ft. Spa, Salon & Fitness Club
- 27-Hole Championship Golf Course, Light-Rail Station (trolley), and San Diego's Largest Premium Mall are all just footsteps away
- 10 short minutes to Attractions, Beaches, the Gaslamp Quarter, Airport, the Arts, Cultural and Sporting Events

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We look forward to having you with us

Town and Country Resort and Conference Center

Hotel Reservation Deadline: September 12, 2014

Official Conference Hotel

Town and Country Resort and Conference Center
550 Hotel Circle North
San Diego, CA 92108 USA

$154+ taxes - single/double

IMAPS 2014 attendees enjoy a special rate of $154+tax per night, single or double occupancy for the premium Royal Palm Tower. Once the Royal Palm Tower has been sold out, IMAPS block guests will be reserved renovated rooms in other towers. **Rooms booked outside of the block for lower rates will not be within the Royal Palm Tower or renovated spaces.**

Reserve your room two ways by the September 12, 2014 discount deadline:

1. **Online reservations link available at www.imaps.org/imaps2014.**
2. **Call 1-800-772-8527 and mention IMAPS to make a reservation by phone.**

IMAPS cannot guarantee room availability and/or rates after the published hotel deadline. Book your rooms directly with the hotel before the deadline noted above.

You spoke and we listened! The Town and Country welcomes IMAPS 2014 with new upgrades.

We heard you in 2012, so IMAPS has acted to reserve the highest quality rooms available for IMAPS 2014. The Town and Country is excited to welcome IMAPS back to its facilities with new and improved service and amenities, including renovated rooms in the premium Royal Palm Tower and complimentary state-of-the-art Wi-Fi in meeting areas. The only way to reserve renovated accommodations is through the block. Lower published rates will reflect accommodations in towers of lesser quality.

Hotel Scams Alert!

The only way to book a room in the official IMAPS Housing Block is using the reservations information provided. All reservations should be made directly with the hotel and within the IMAPS room block.

IMAPS does not utilize the services of a housing company. If any person or firm contacts you and offers to handle your reservations, please beware. They are completely unauthorized and possibly fraudulent. The convention industry is currently plagued by such groups. If you use one of them and experience any problems, including lost deposits and no reservation when you arrive, IMAPS may not be able to assist you. Please be aware in particular of one of these unauthorized firms - Exhibition Housing Services - whose salespeople have falsely claimed to be calling from IMAPS.

Registration

Early Registration & Hotel Deadline: September 12, 2014

Three Convenient Ways to Register

1. **Online: www.imaps2014.org**
2. **Mail form to:**

   IMAPS 2014 Registration
   P.O. Box 110127
   Research Triangle Park, NC 27709-0165 USA

   For more information, please call IMAPS
   +1-919-293-5000
3. **Fax: +1-919-287-2339**

Save Time! Register Online: www.imaps2014.org

Advance Registration

To register in advance for IMAPS 2014, your registration and payment information must be received no later than September 12, 2014. Register early and save $100. All registrations received after September 12, 2014, will be considered "on-site registration." Confirmations will be sent upon processing of registration form and payment. Those who register in advance may proceed on-site to Advance Registration to retrieve their badge and Proceedings USB at the Symposium.

International Wire Transfers

For wire transfer information, e-mail Michael O'Donoghue (modonoghue@imaps.org) or call 1-919-293-0550.

A $25 fee must be added to all Wire Transfers.

Full Symposium Cancellation Policy

Registration cancellations will be refunded (less a $100 processing fee) only if written notice is postmarked on or before September 12, 2014. No refunds will be issued after that date. No shows will not be eligible for refunds.

Photo Release

Photographs will be taken at the IMAPS 2014 Symposium. By registering for this meeting, you agree to allow IMAPS to use your photo in any IMAPS-related publications or website.

Loss Due to Theft

Symposium management is not responsible for loss or theft of personal belongings. Security for personal belongings is the responsibility of the individual.

Full attendee registrations (not exhibits only) includes the Opening Ceremonies, IMAPS Annual Business Meeting, IMAPS Awards Ceremony, Keynote Presentations, Welcome Reception, Technical Sessions, GBC-Marketing Forum, Panel Discussion, Exhibit attendance, Breaks, Exhibit Hall Reception on Wednesday, Exhibit Hall Lunch on Tuesday, one 2014 Proceedings USB and an automatic one-year IMAPS membership renewal for individual and student members in good standing at the time of registration. For an additional fee you can register for a Professional Development Course (PDC), the Golf Tournament, and other activities/purchases.

Town & Country Resort and Conference Center

550 Hotel Circle North
San Diego, CA 92108 USA

$154+ taxes - single/double

Reserve your room two ways by the September 12, 2014 discount deadline:

1. **Online reservations link available at www.imaps.org/imaps2014.**
2. **Call 1-800-772-8527 and mention IMAPS to make a reservation by phone.**

Full Symposium Registration

Your Full Symposium registration includes the following:

WR Welcome Reception
KP Keynote Presentations
EL Exhibits Hall Buffet Lunch
TS Technical Sessions
EX Exhibits
PR One USB Proceedings

✓	Type (check one)	Includes	Advance (on/before 9/12)	On-site (after 9/12)
	IMAPS Member*	WR, KP, EL, TS, EX, PR	$650	$750
	Non-member*	WR, KP, EL, TS, EX, PR	$790	$890
	Presenters/Speakers*	WR, KP, EL, TS, EX, PR	$530	$630
	Session Chair/Co-chair*	WR, KP, EL, TS, EX, PR	$530	$630
	Chapter Officers*	WR, KP, EL, TS, EX, PR	$530	$630
	Student Member*	WR, KP, EL, TS, EX, PR	$30	$40
	Student Non-member*	WR, KP, EL, TS, EX, PR	$35	$45
	Exhibits Only Tuesday	KP, EX (lunch not included)	FREE	FREE
	Exhibits Only Wednesday	KP, EX (lunch not included)	$35	$40
Includes one-year individual membership or individual membership renewal at no additional charge.				
	Additional Events			
	Golf Tournament (Team of 4)		$125 (1 golfer) $450 (4-some)	
	Golf Tournament (One Golfer including 1 hole sponsorship)		$500	
	Golf Tournament (Team of 4 including 1 hole sponsorship)		$750	
	Tuesday, October 14 Exhibit Hall Lunch Ticket 12:45-2:00		$35	

#1 Subtotal Symposium Registration $_____

Professional Development Courses

Monday, October 13: full-day courses (M1-6), running 10:00 am - 6:00 pm;
Monday, October 13: half-day courses running 10:00am - 1:45pm (MA1-4) & 2:15 pm - 6:00 pm (MP1-3)
Thursday, October 16: All courses are half-day (T1-6), running 8:00 am - 12:00 pm

	✓	Course Title	Advance (on/before 9/12)	On-site (after 9/12)
M1		Intro to 3D Printed Power Electronics…	$600	$700
M2		Intro to Design and Fabrication of RF…	$600	$700
M3		Intro to Microelectronics Packaging	$600	$700
M4		Polymer Challenges in Packaging…3D	$600	$700
M5		Technology of Screen Printing	$600	$700
M6		Wire Bonding	$600	$700
MA1		ENIG Plating for Electronics…	$400	$500
MA2		High-Temperature Electronics	$400	$500
MA3		MEMS and nanoMEMS…	$400	$500
MA4		Package level integration: 2D, 2.5D & 3D…Mobile Systems	$400	$500
MP1		Low-Temperature Electronics	$400	$500
MP2		Package on Package Technology…	$400	$500
MP3		Thermal & Mech Simulation Techniques…	$400	$500
T1		Chip Packaging Processes and Materials	$400	$500
T2		Fundamentals of Micro Packaging	$400	$500
T3		IC Fabrication…Packaging	$400	$500
T4		Interposers - Silicon, Organic and Glass	$400	$500
T5		Packaging & Testing of Implanted Medical Devices	$400	$500
T6		Common Failure Modes from a Physics of Failure Perspective	$400	$500

#2 Subtotal PDC Registration $_____

Exhibit Booth Purchase

❑ 10'x10' Exhibit Space
$2000 members, $2600 non-members

❑ 10'x20' Exhibit Space
$3300 members, $3900 non-members

Other sizes available
visit www.imaps2014.org for information.

No. of Booths _____ @ $ _____ each
Total $ _____

Company Name

_____

Contact Name

_____

#3 Subtotal Exhibit Registration
$_____

Additional Purchases

A Full Symposium Registration includes 1 copy of the Proceedings USB only. **You must pick-up your Proceedings at the registration desk.**

❑ Extra IMAPS 2014 USB Proceedings
USB only: $225 members, $325 non-members*
Add $7 to ship in the US; Add $25 to ship Overseas
Qty. _____ $ _____

#4 Subtotal Proceedings Registration
$_____

Foundation Contribution

IMAPS Microelectronics Foundation Contribution
$ _____

#5 Subtotal Foundation Donation
$_____

Early Registration/Hotel Deadlines: September 12, 2014

IMAPS cannot guarantee room availability and/or rates after the published hotel deadline. Book your rooms directly with the hotel before the deadline noted above. *See Registration on Pages 57-58.*

Tell Us About Yourself *(please print)*

Early Registration/Hotel Deadlines: September 12, 2014

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❑ Mr. ❑ Ms. ❑ Dr. IMAPS ID#_____

First _____

Last _____

Position/Title _____

Company/University _____

Address _____

City _____ State _____ Zip/Postal Code _____

Country _____

Phone (_____) _____ Fax (_____) _____

E-mail _____

(Email address required to receive confirmation of registration.)

Companion Information (if attending)

❑ Mr. ❑ Ms. ❑ Dr.

First _____ Last _____

City _____ State _____

Zip/Postal Code _____ Country _____

How did you hear about this Event? (please check all that apply)

❑ Direct Mail ❑ Advancing Microelectronics ❑ Website ❑ E-mail

❑ Personal Phone Call ❑ Industry/Trade Magazine ❑ Colleague ❑ IMAPS Weekly E-mail Bulletin

Other _____

Hotel: Are you staying at the host hotel? (Attendees are responsible for reserving their own hotel room, see pages 56-57 for details.)

❑ Town and Country Resort ❑ I'm staying at another Hotel ❑ Local

(name) _____

Total Fees and Deposits

#1 Symposium Registration Subtotal $_____

#2 PDC Registration Subtotal $_____

#3 Exhibit Booth Purchase Subtotal $_____

#4 Additional Purchases Subtotal $_____

#5 Foundation Contribution Subtotal $_____

TOTAL AMOUNT DUE $_____

❑ Enclosed check payable to IMAPS - Check #_____

Charge My Fees to:

❑ Visa ❑ MasterCard ❑ Discover ❑ American Express

Card#_____ Exp._____

Cardholder Name _____

Signature _____

Cardholder address if different than above: (required)

_____

_____

Full Symposium cancellations will be refunded (less a $100 processing fee) only if written notice is postmarked on or before Friday, September 12, 2014. **No refunds will be issued after that date.**

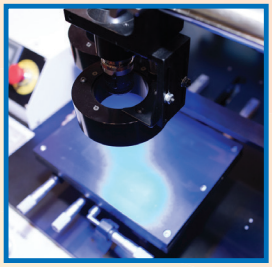
IMAPS 2014 Registration
P.O. Box 110127
Research Triangle Park, NC 27709-0165

Early Registration & Hotel Deadline: September 12, 2014

47th International Symposium on Microelectronics

October 13-16, 2014

Town & Country Resort and Conference Center • San Diego, CA



IMAPS2014.org